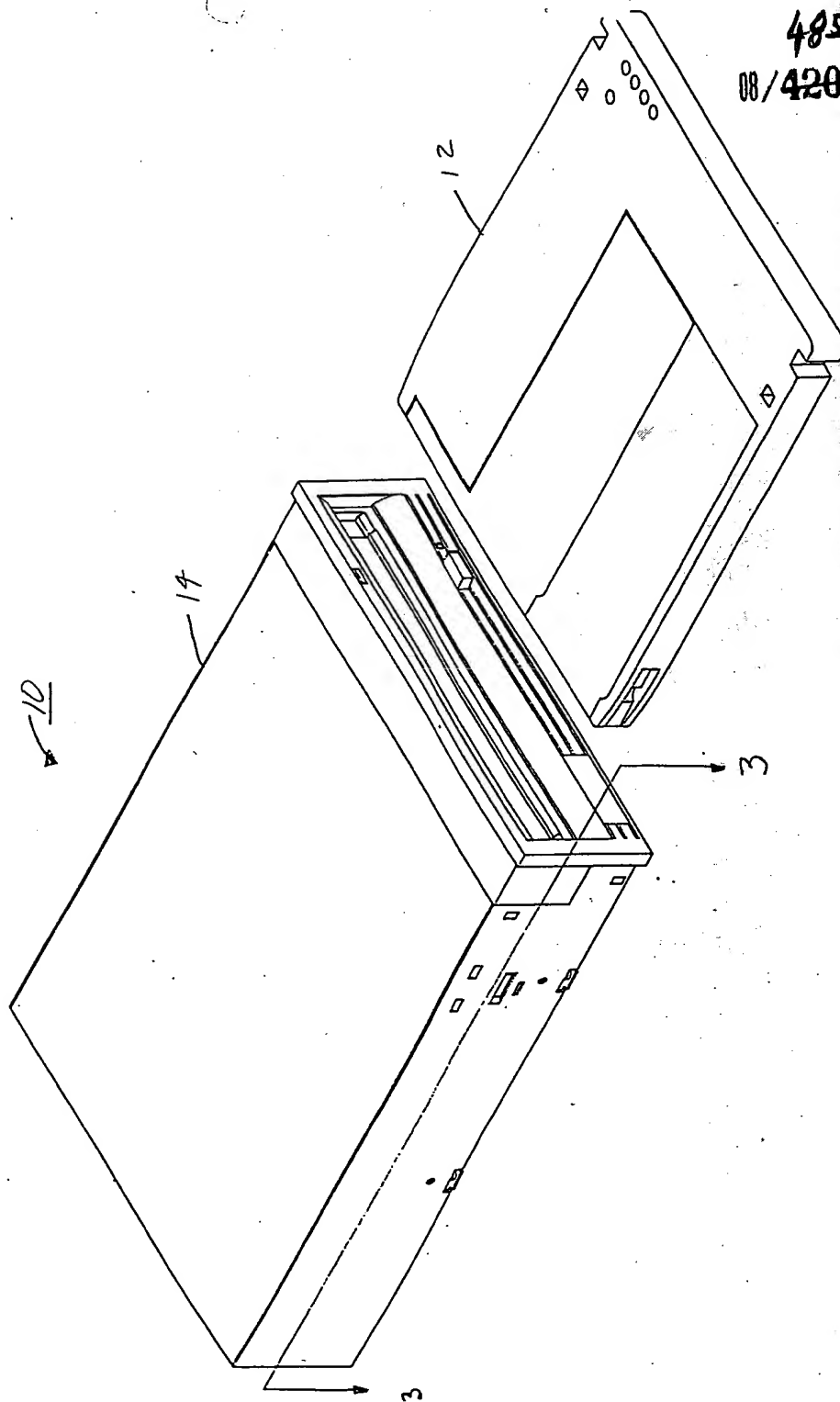


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T. Dinh

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FIG. 1

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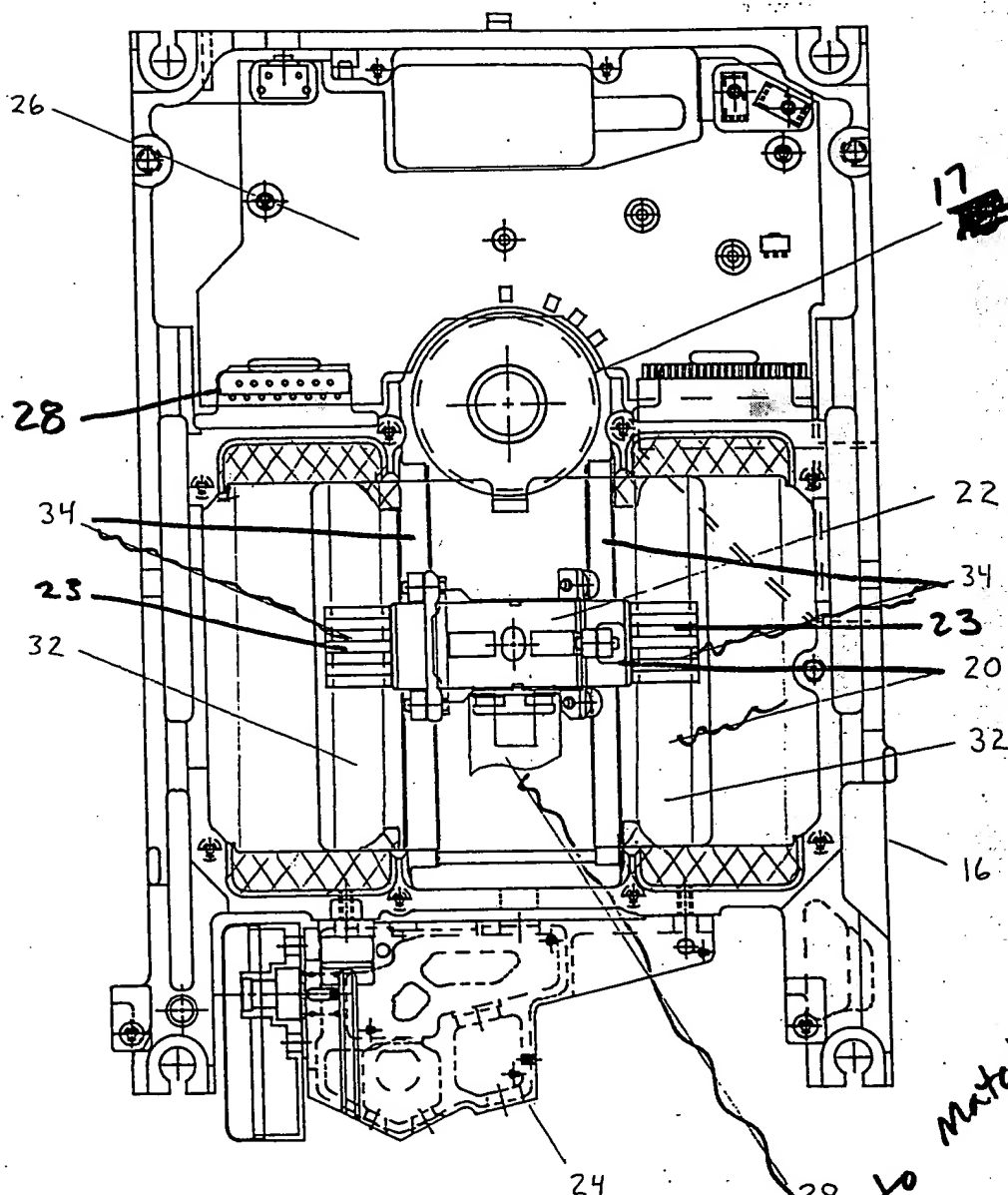


FIG. 2

Re-do to match
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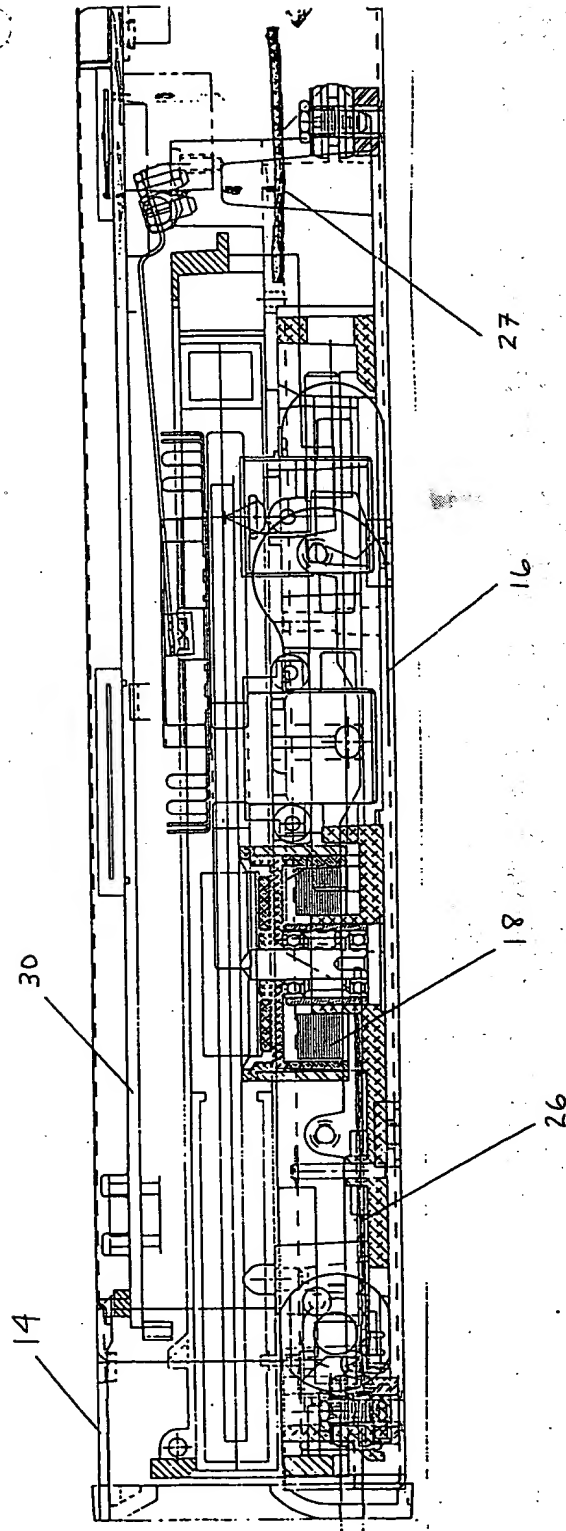
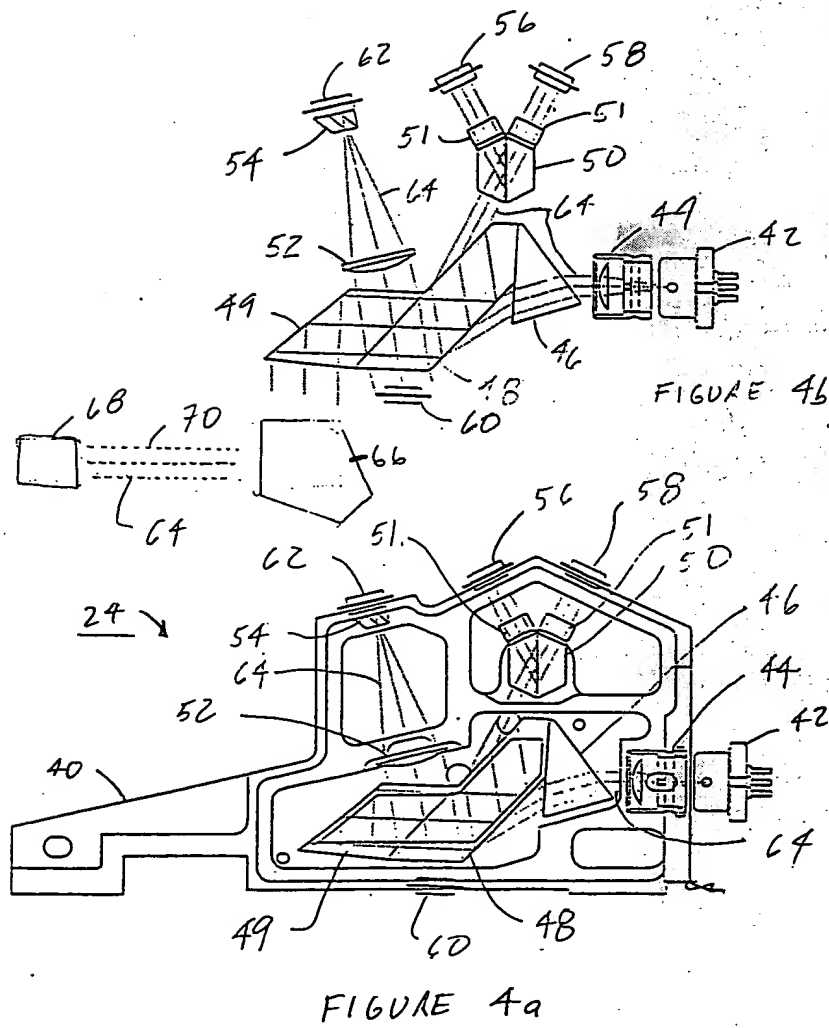


FIGURE 3

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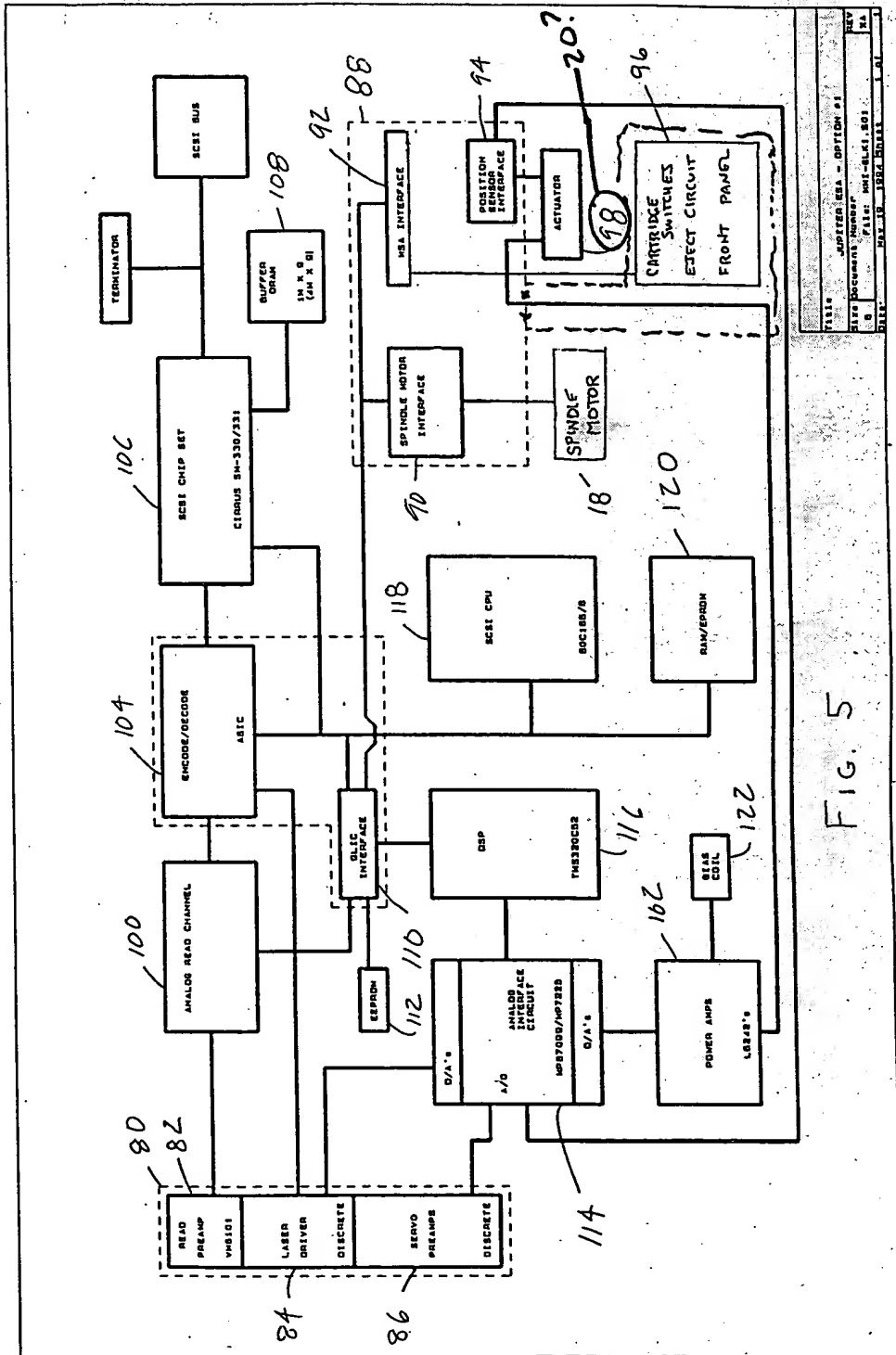


FIG. 5

FILE	ADPTEP SEA - OPTION 91
REV	1
DATE	10/1/82
BY	WJL
CHKD	WJL
FILE	WJL-SEA-001
DATE	10/1/82
BY	WJL
CHKD	WJL

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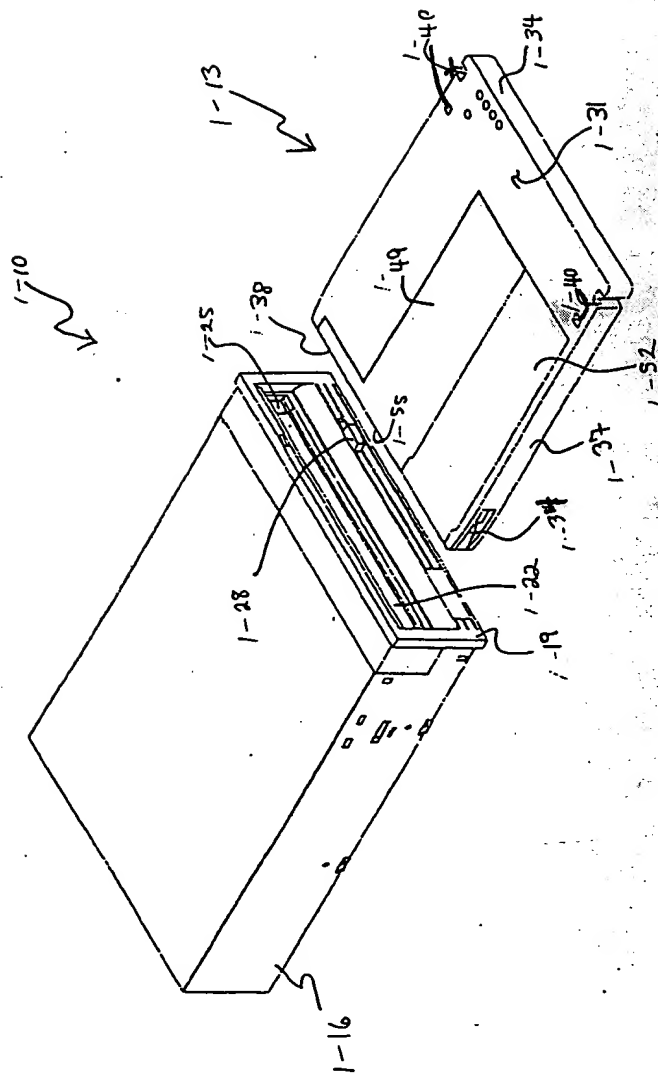


FIG. 10

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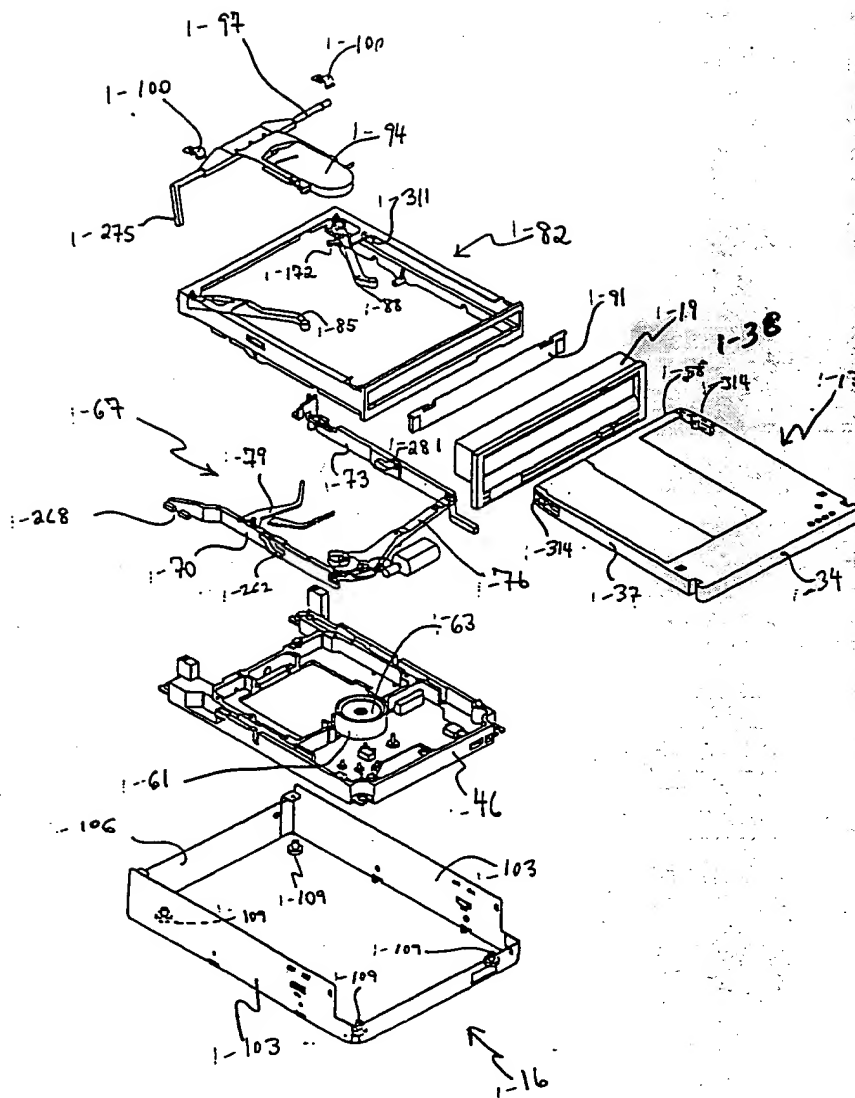


FIG. 2

08/420899

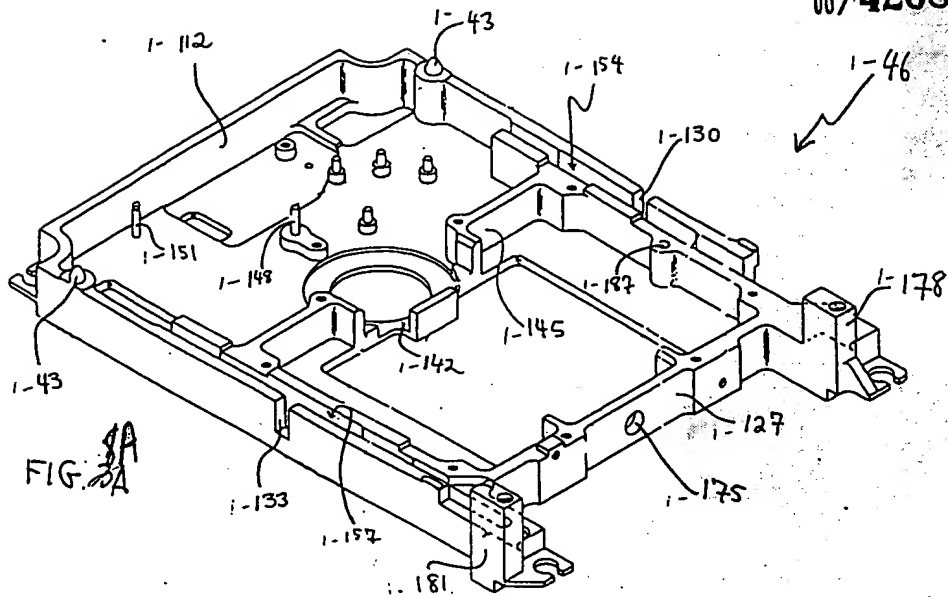


FIG. 3A

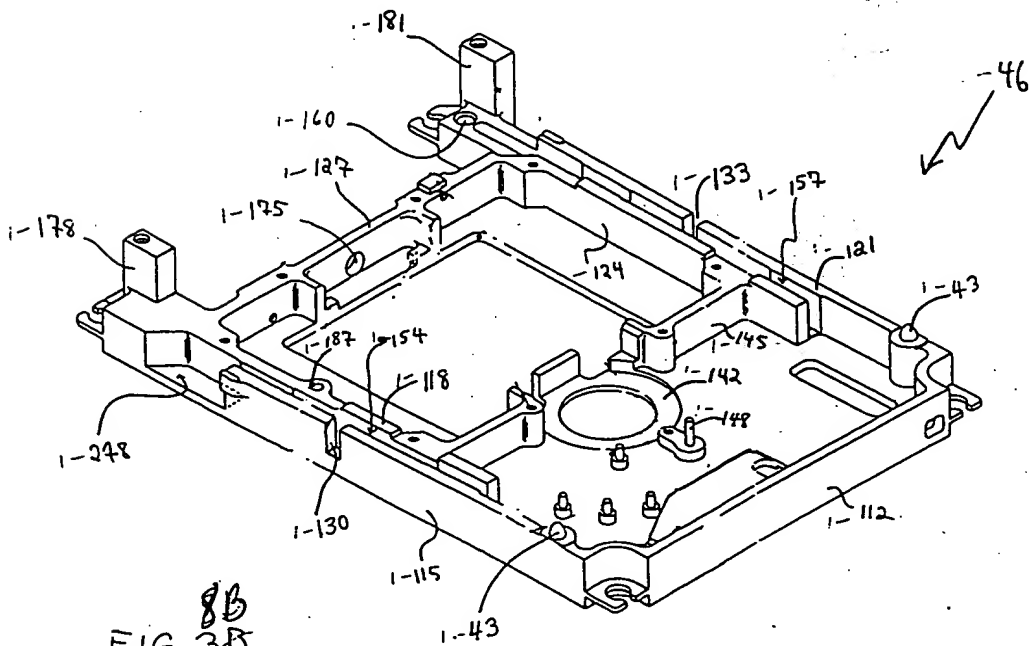
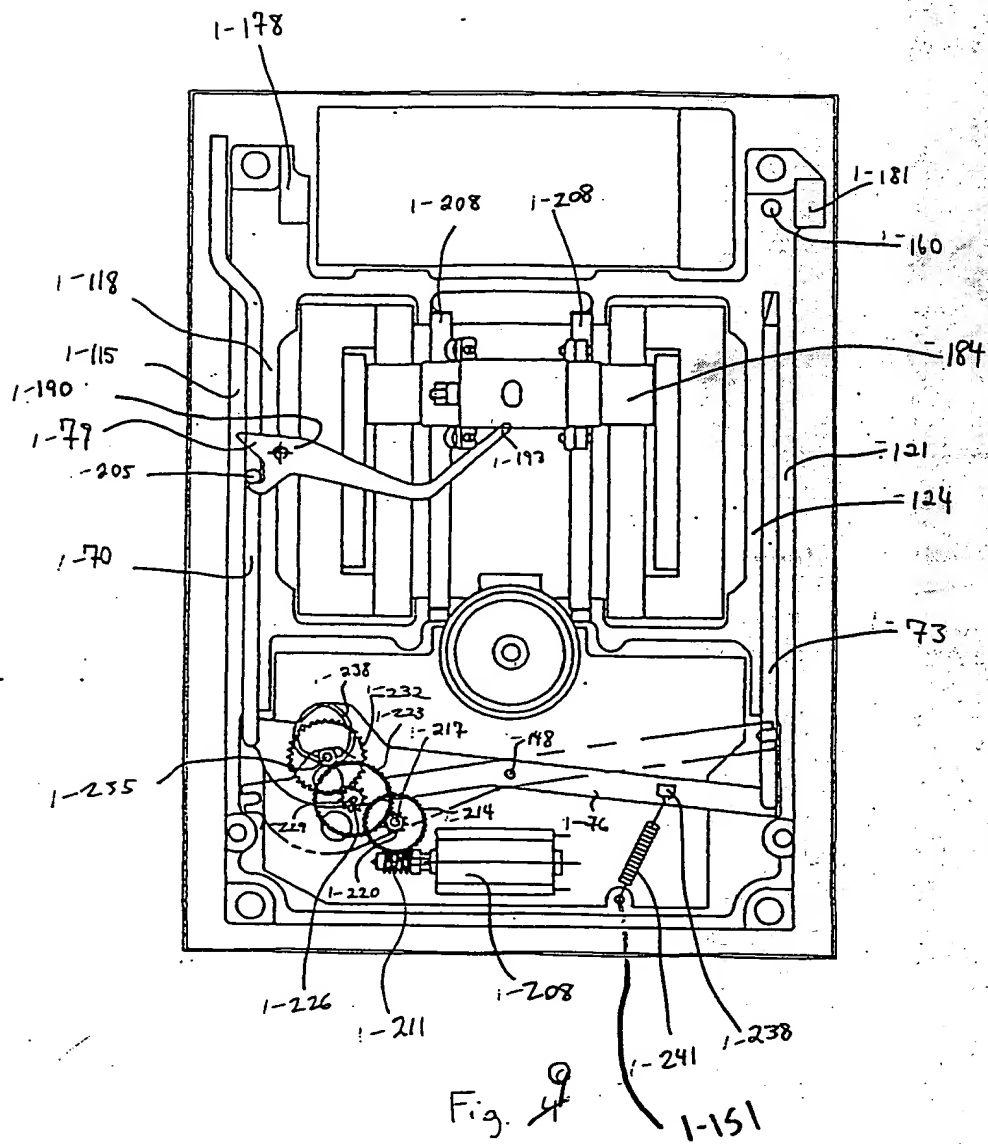


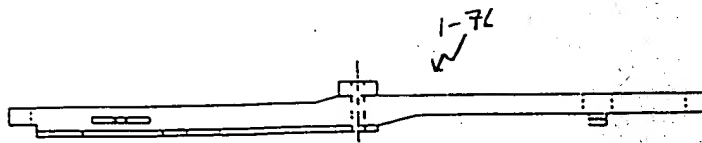
FIG. 3B

08/420899

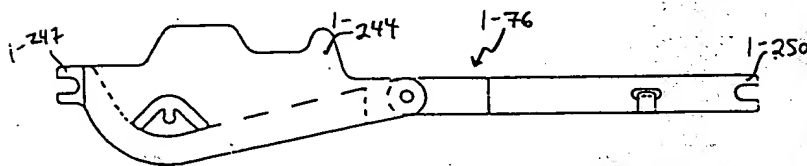


08/420899

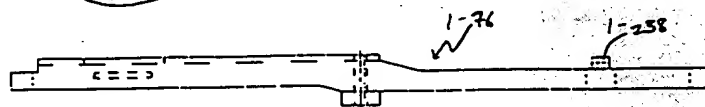
10A
FIG. 5A



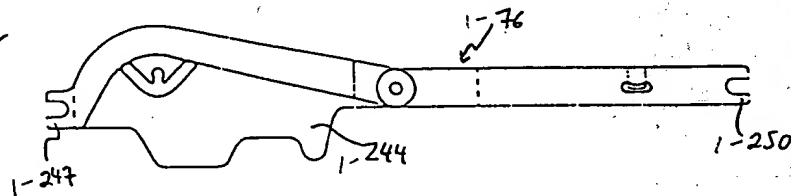
10B
FIG. 5B



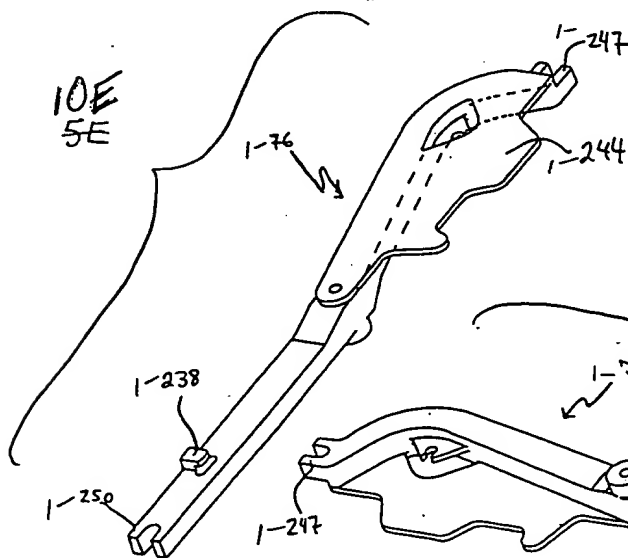
10C
FIG. 5C



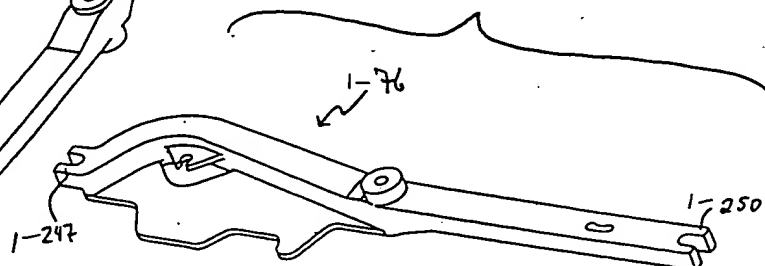
10D
FIG. 5D



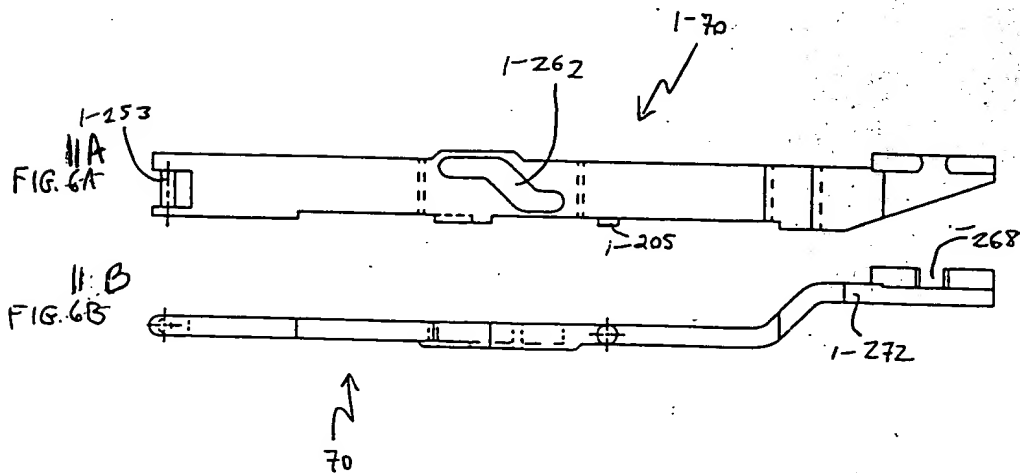
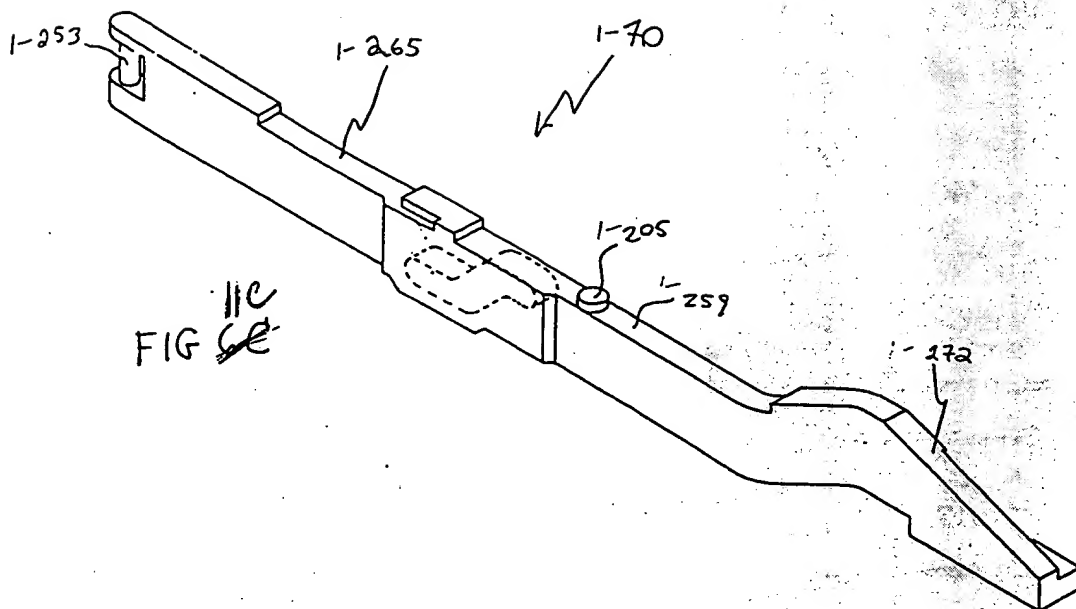
10E
5E



10F
5F

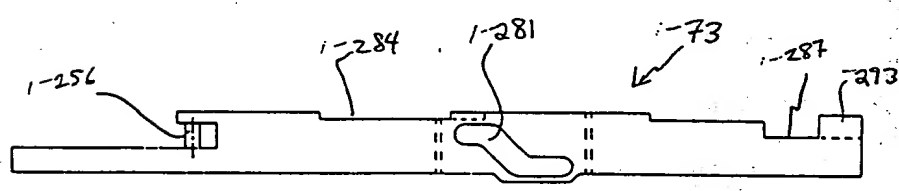
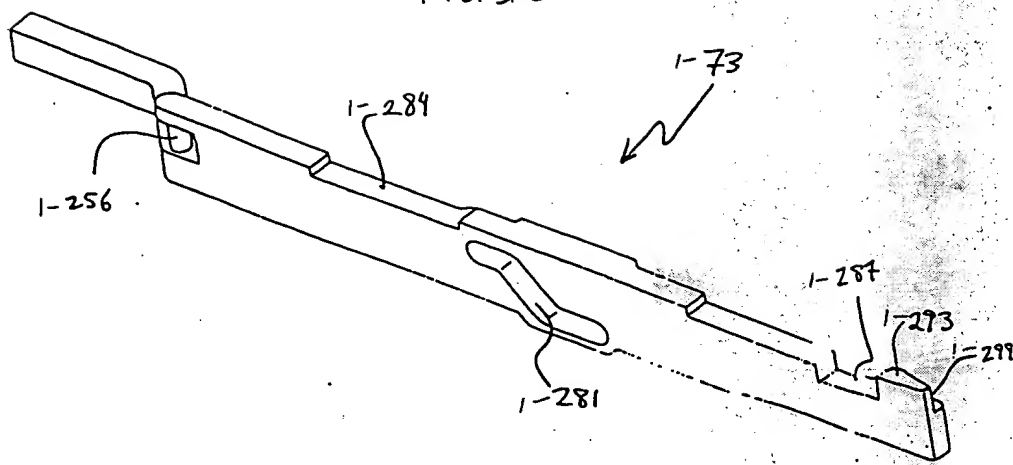


08/420899

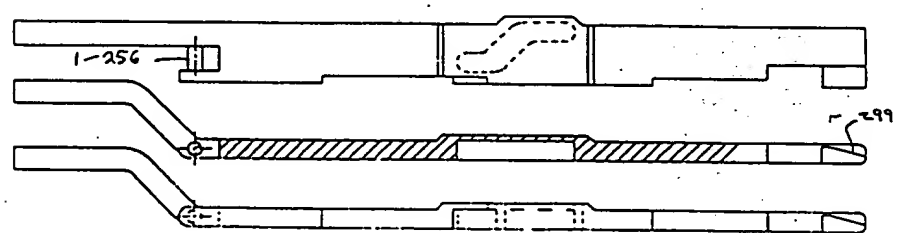


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12E
FIG. 7E



12A
FIG. 7A



12B
FIG. 7B

12C
FIG. 7C

12D
FIG. 7D

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FIG. 13C
~~8C~~

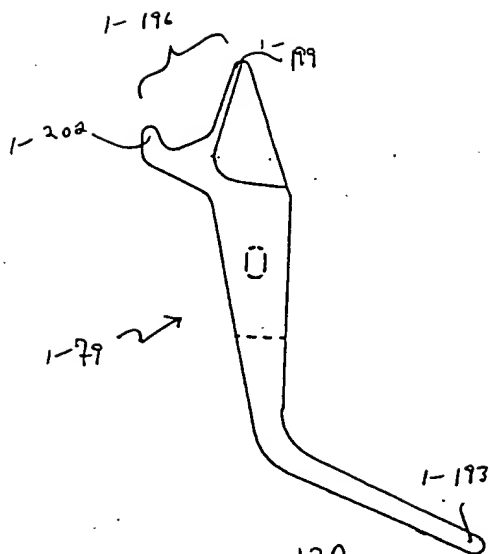
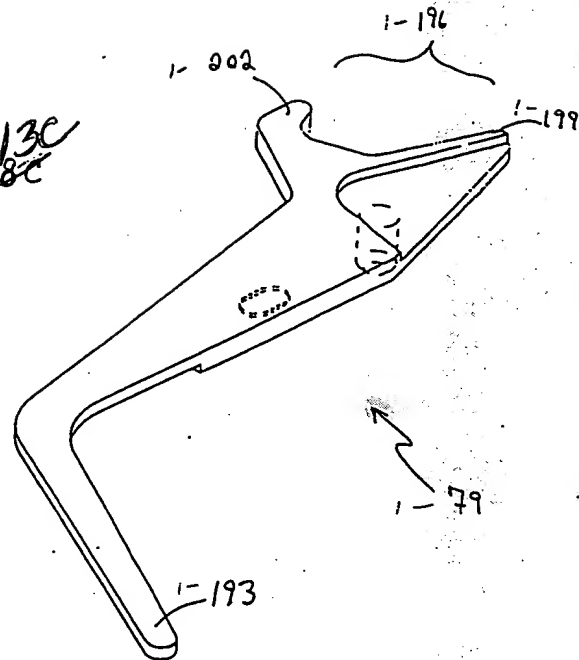


FIG. 13A
~~8A~~

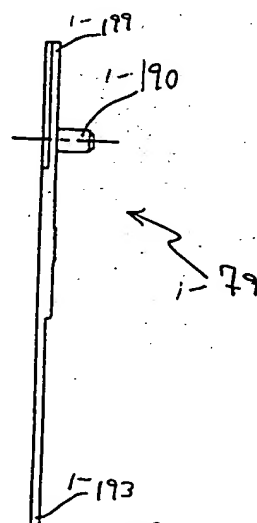
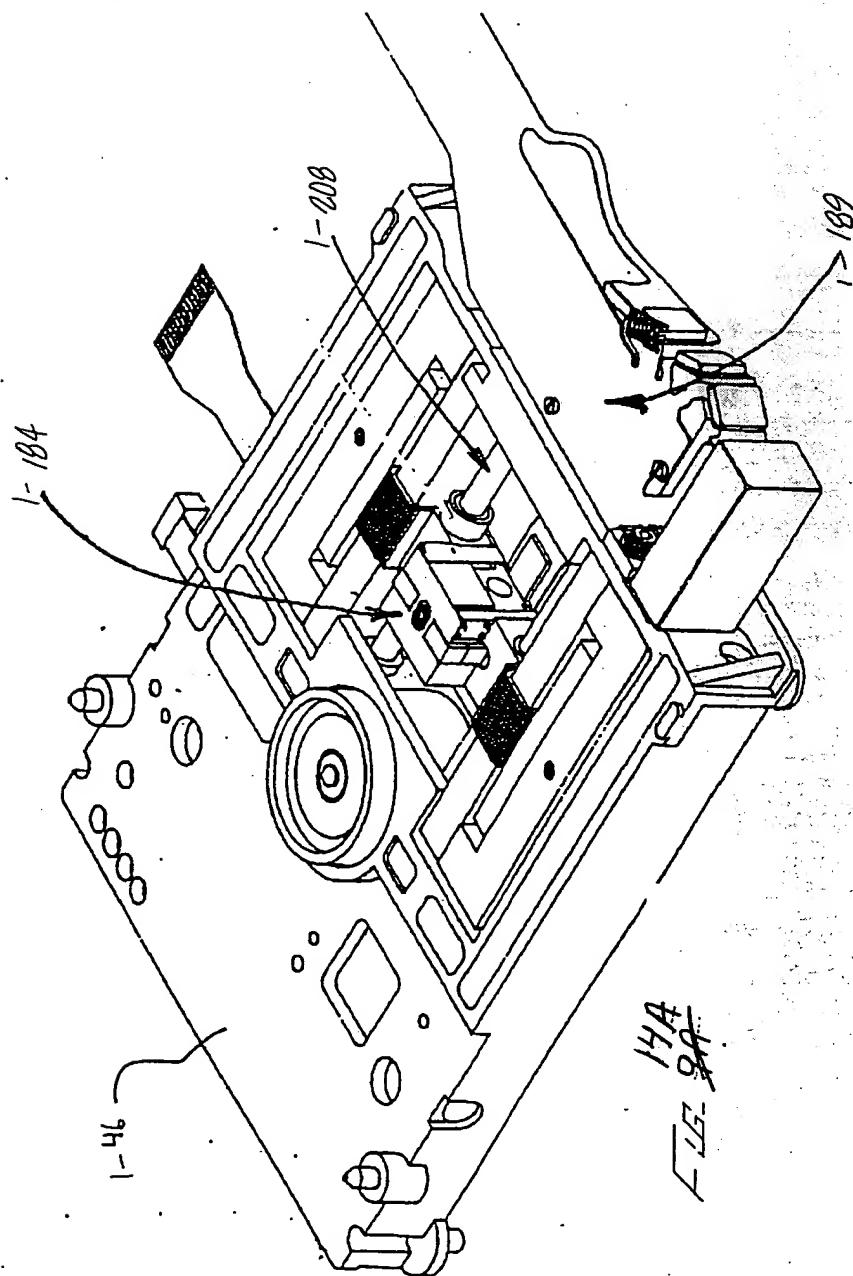


FIG. 13B
~~8B~~

08/420899



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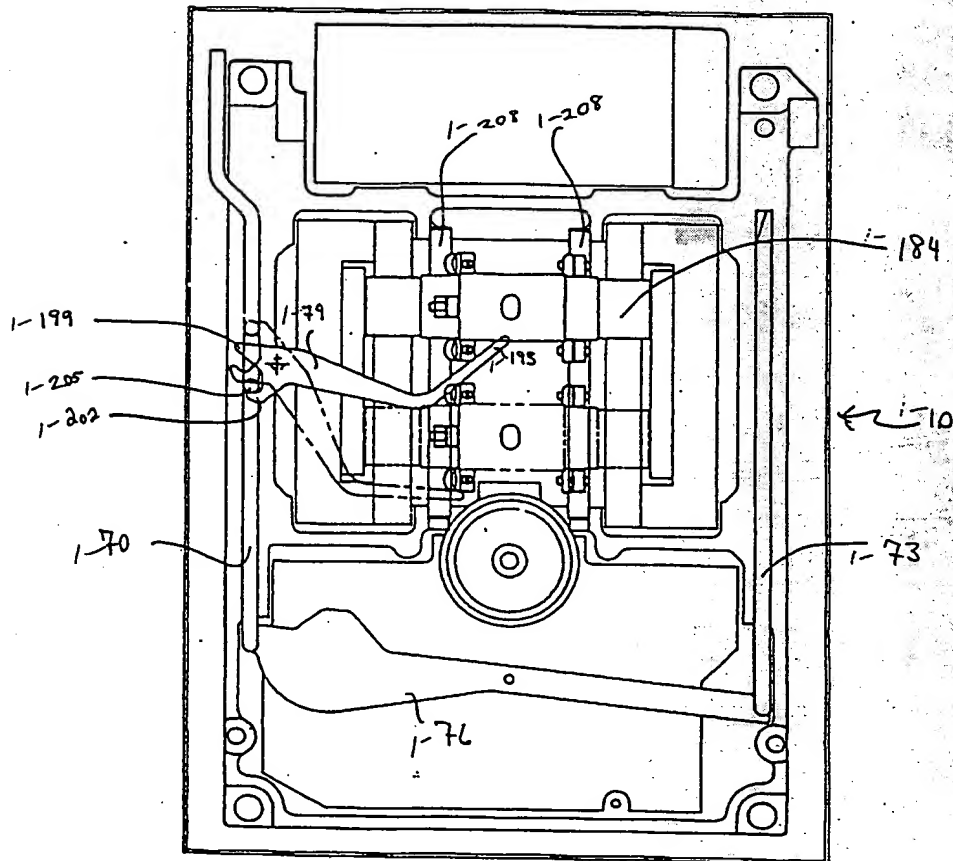


FIG. 14B
~~9B~~

08/420899

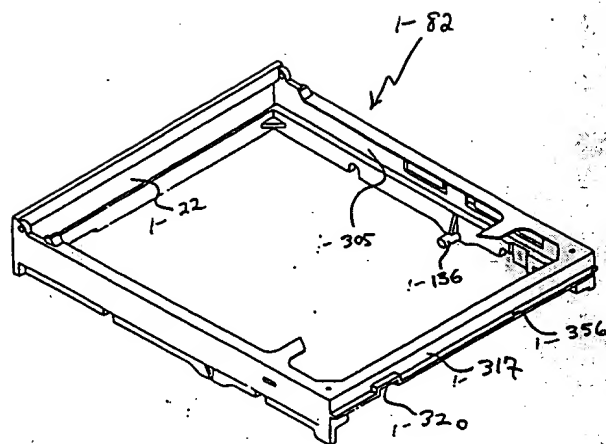


FIG. 15A
10A

16

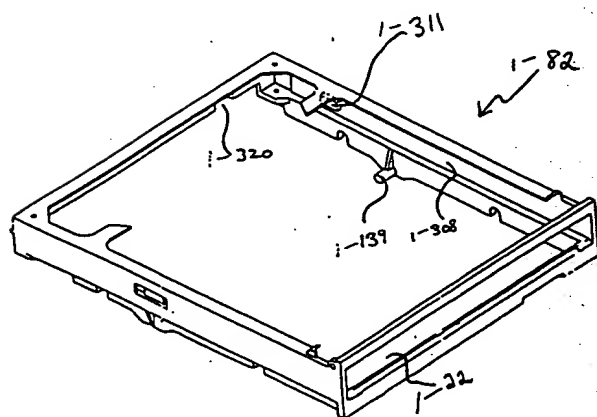


FIG. 15B
10B

08/420899

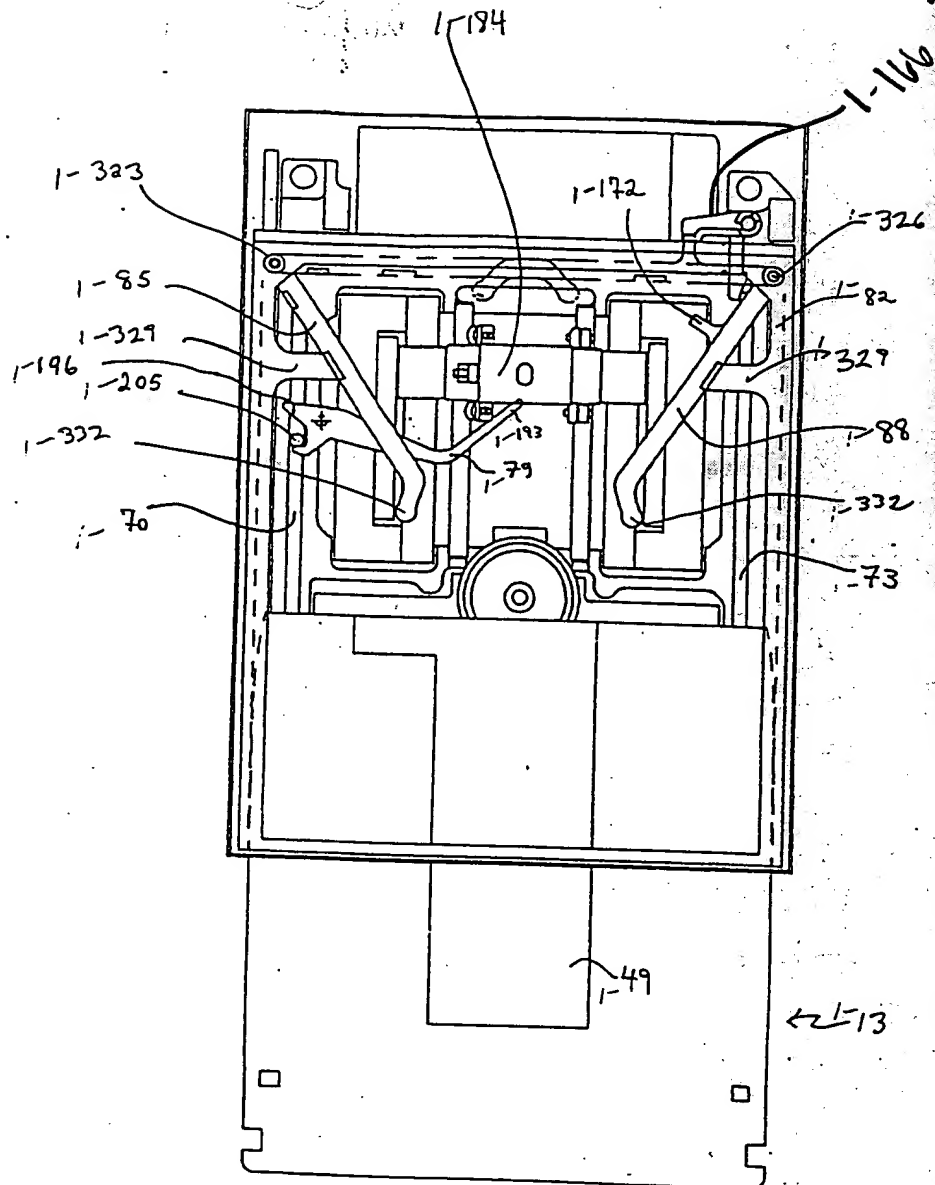


FIG. 16A

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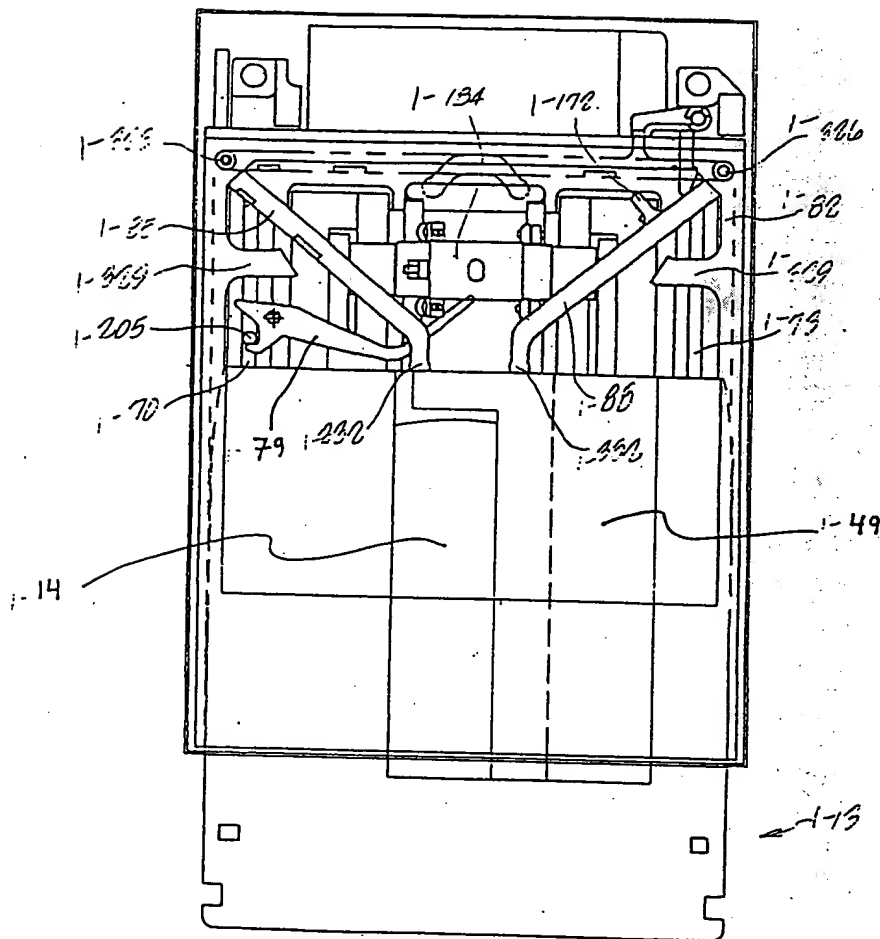


FIG. 16B

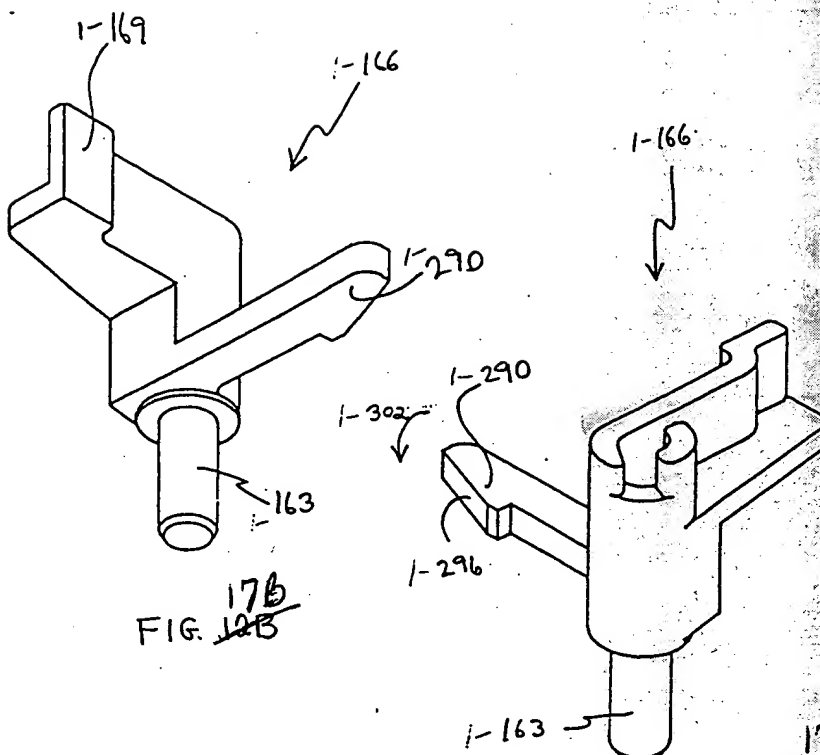


FIG. 17B

FIG. 17A

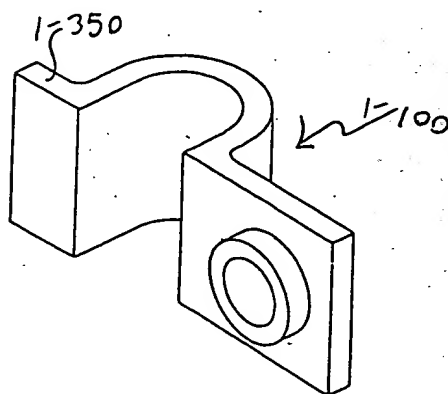


FIG. 18

08/420899

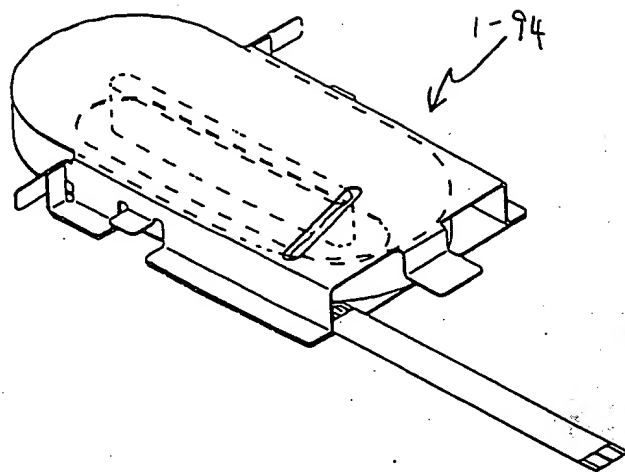


FIG. 19

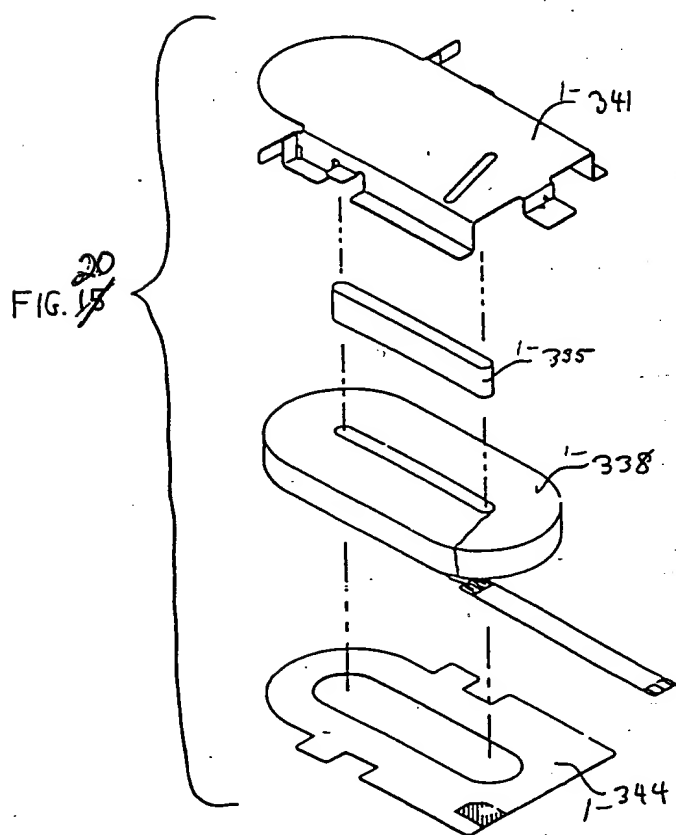
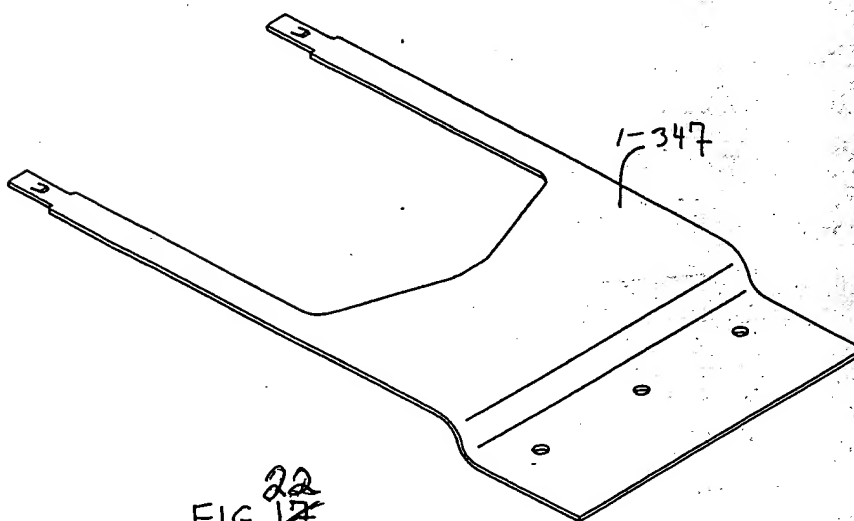
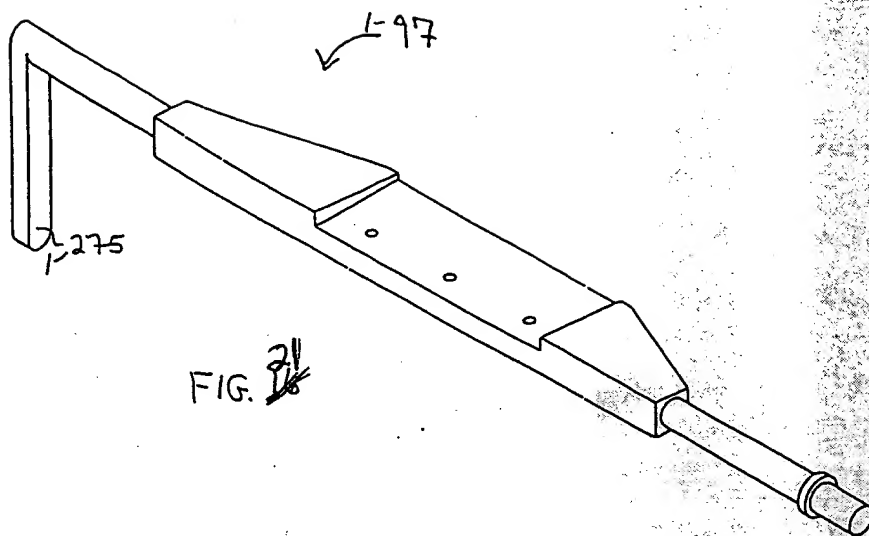


FIG. 20

08/420899



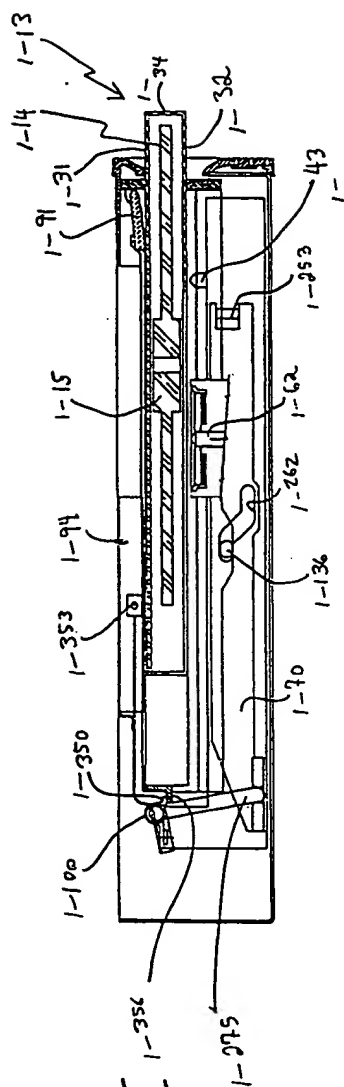


FIG. 25

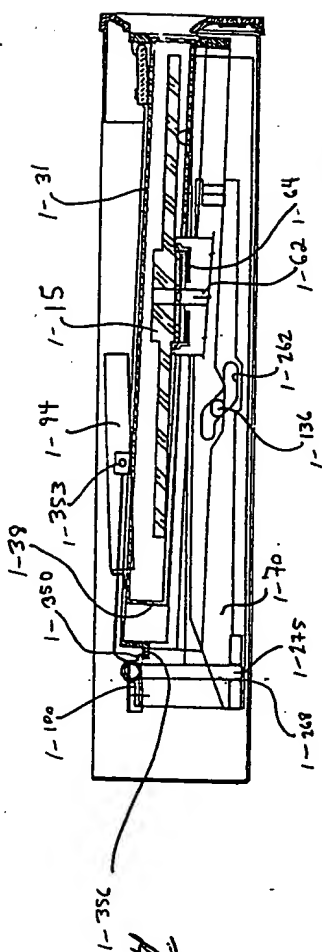


FIG. 24

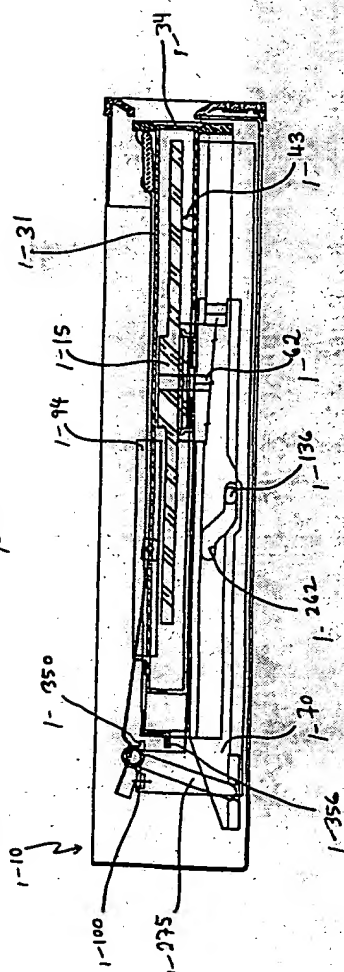


FIG. 23

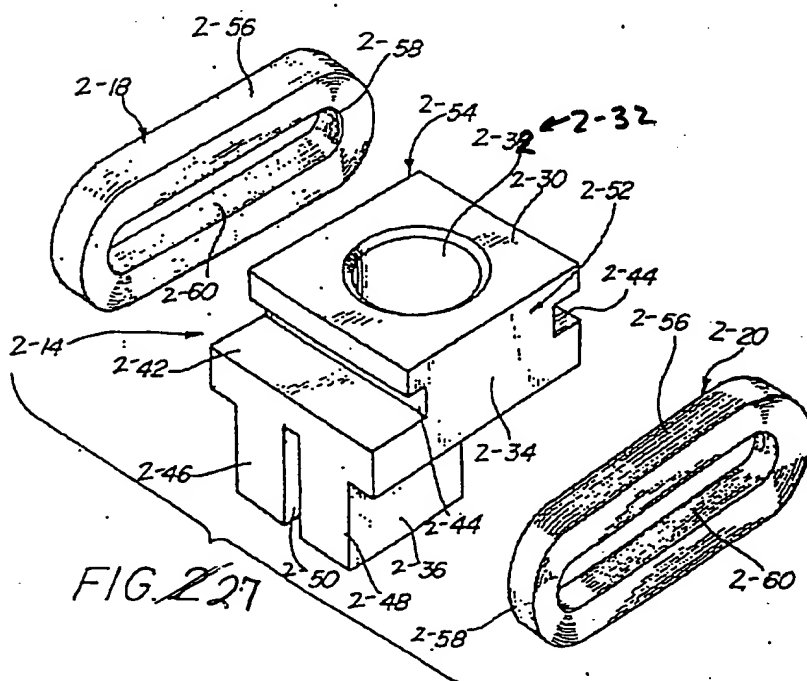
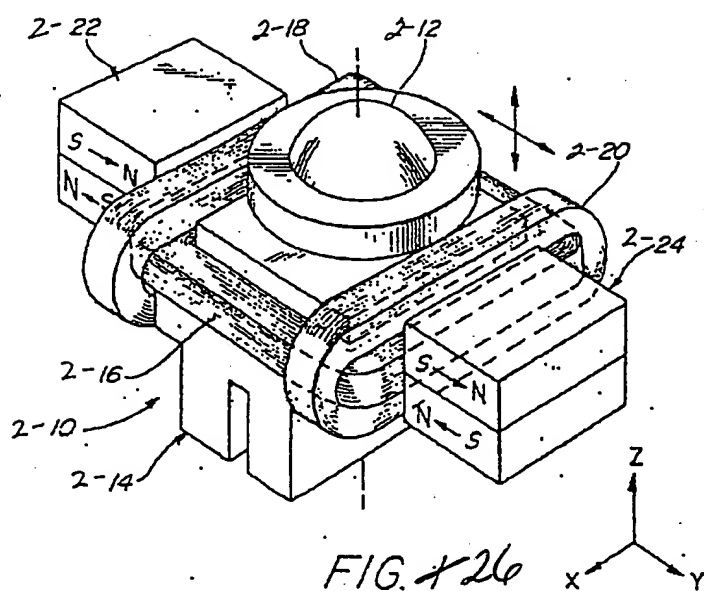
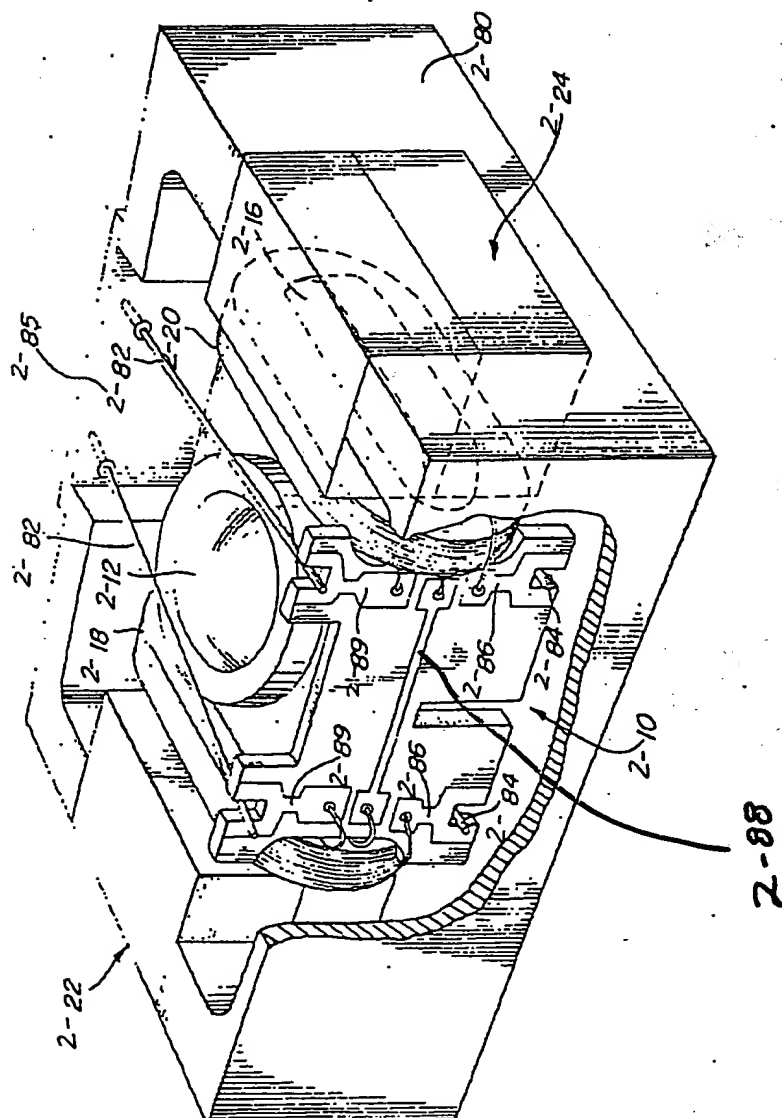


FIG. 3/28



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FIG. 4 29

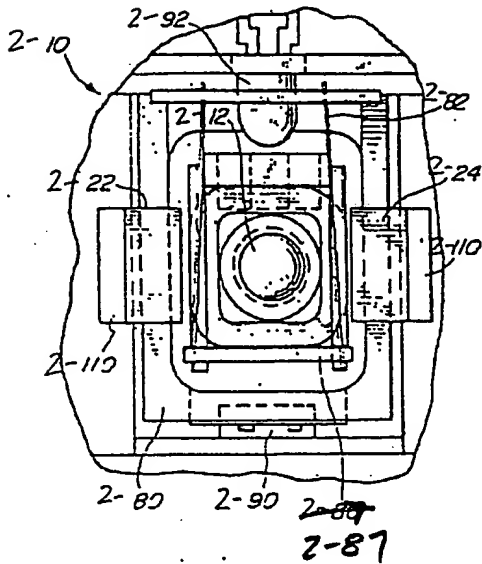


FIG. 5 30

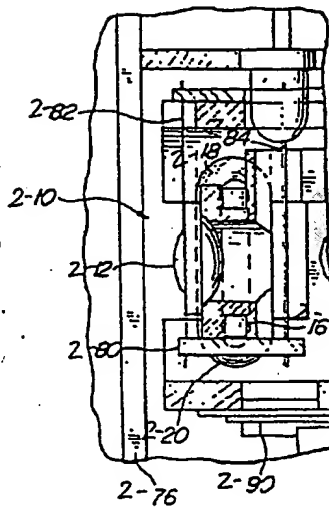
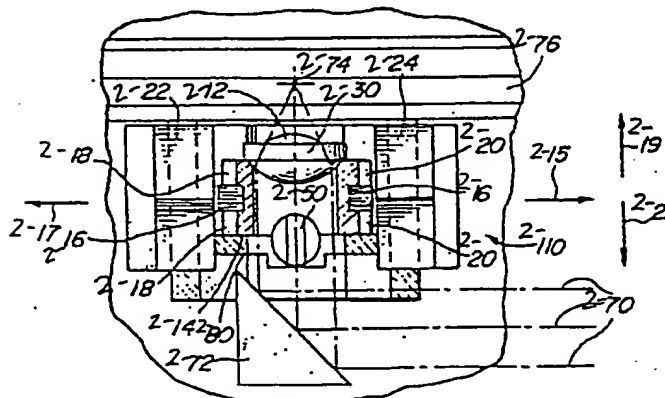


FIG. 6 31



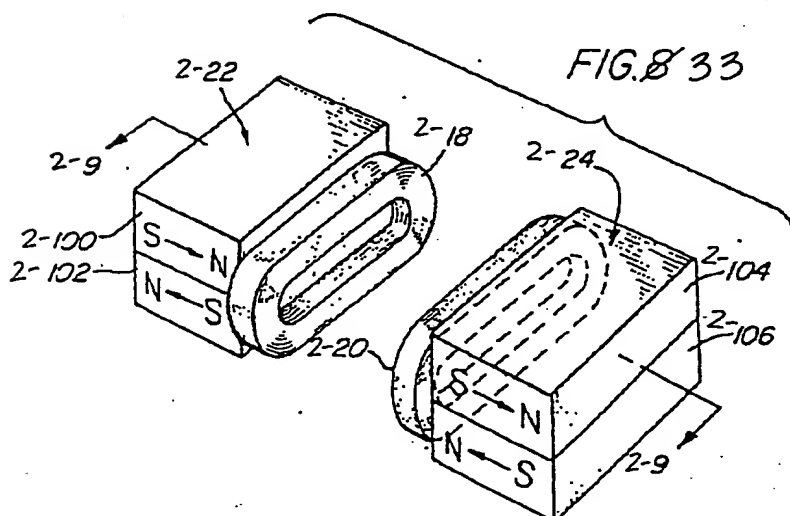
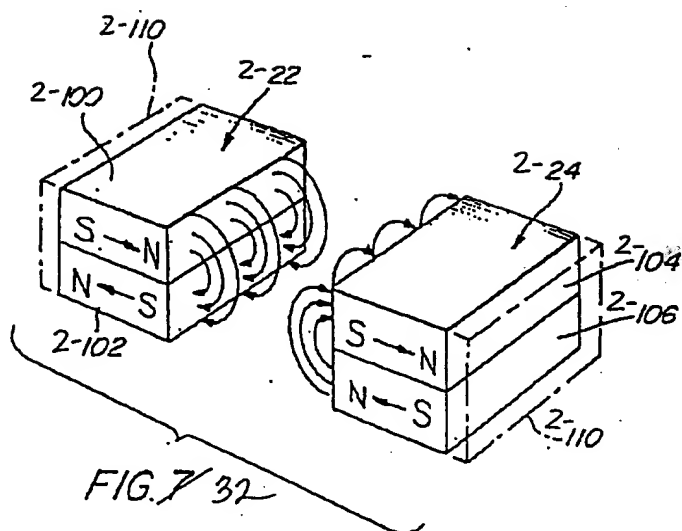


FIG. 9 34

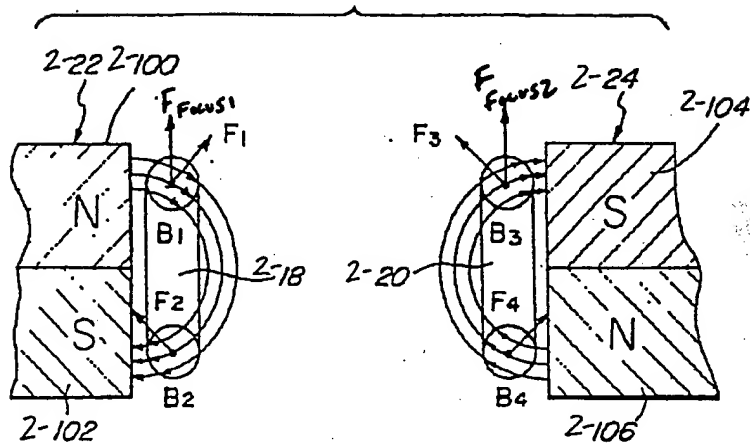
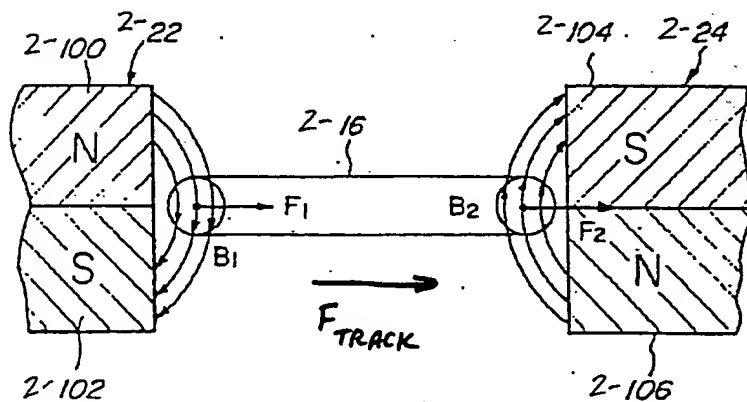
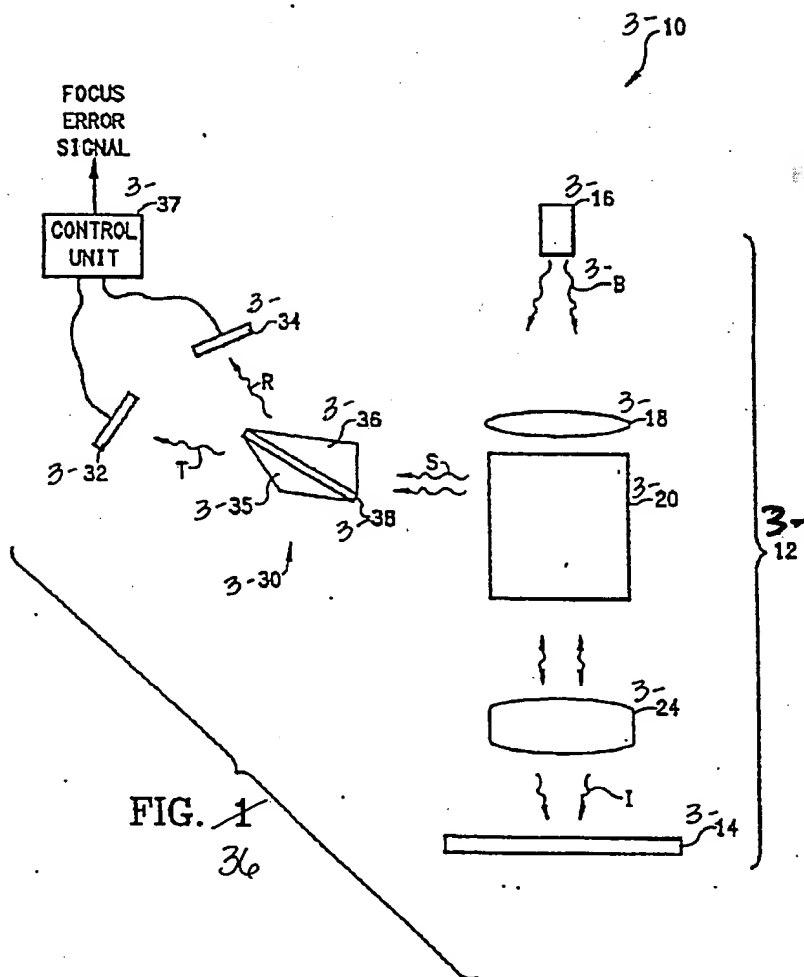


FIG. 10 35





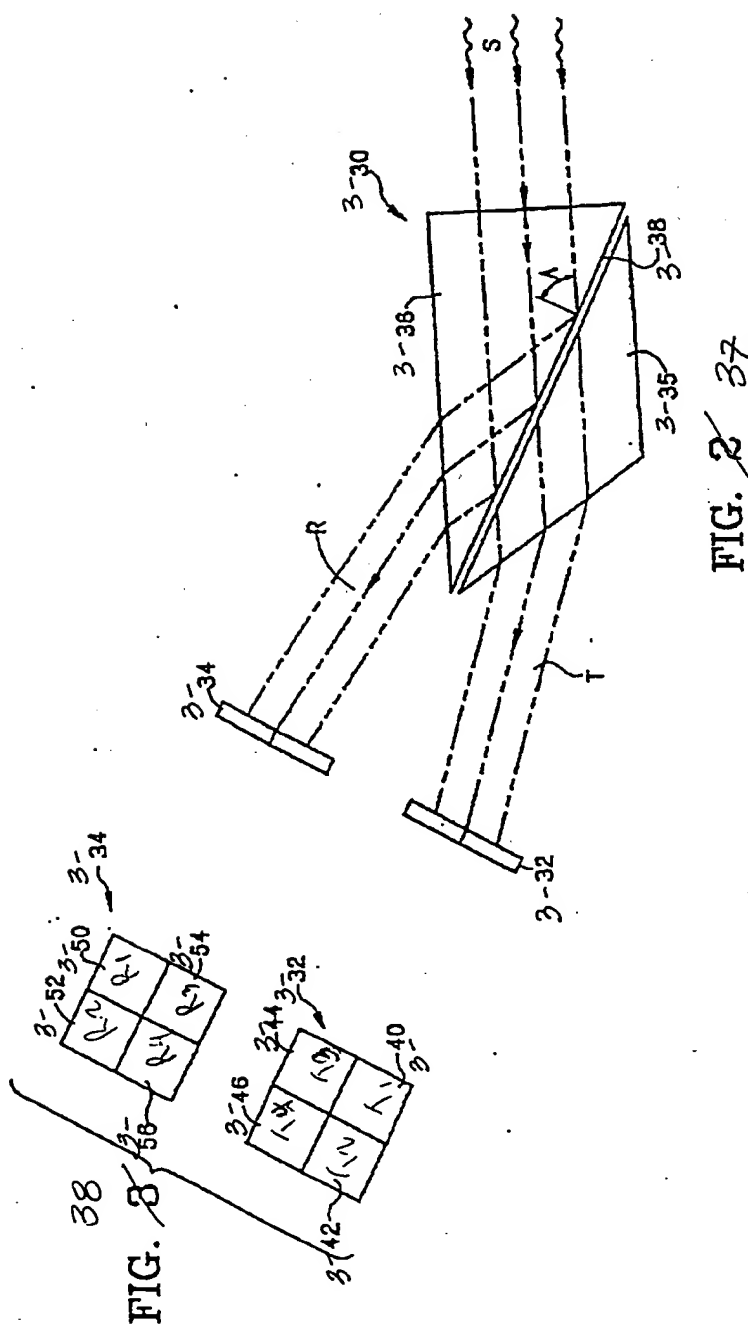


FIG. 4 39

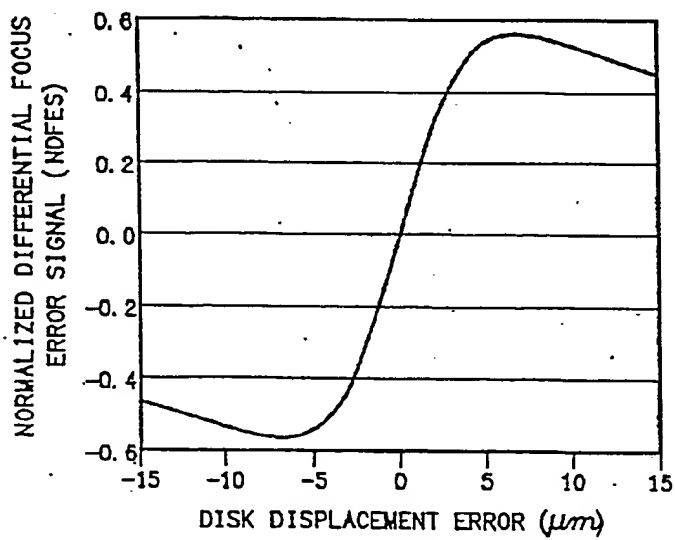
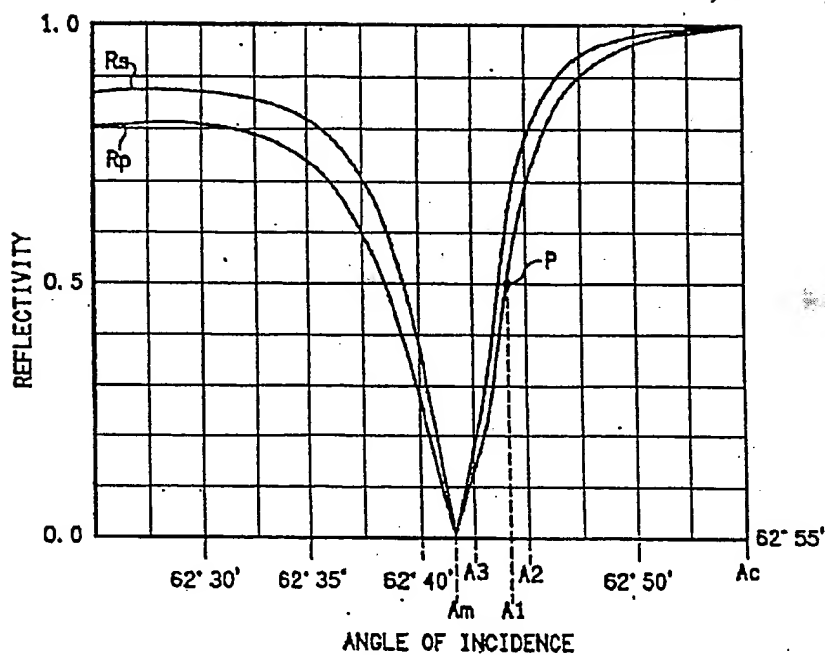


FIG. 5 40

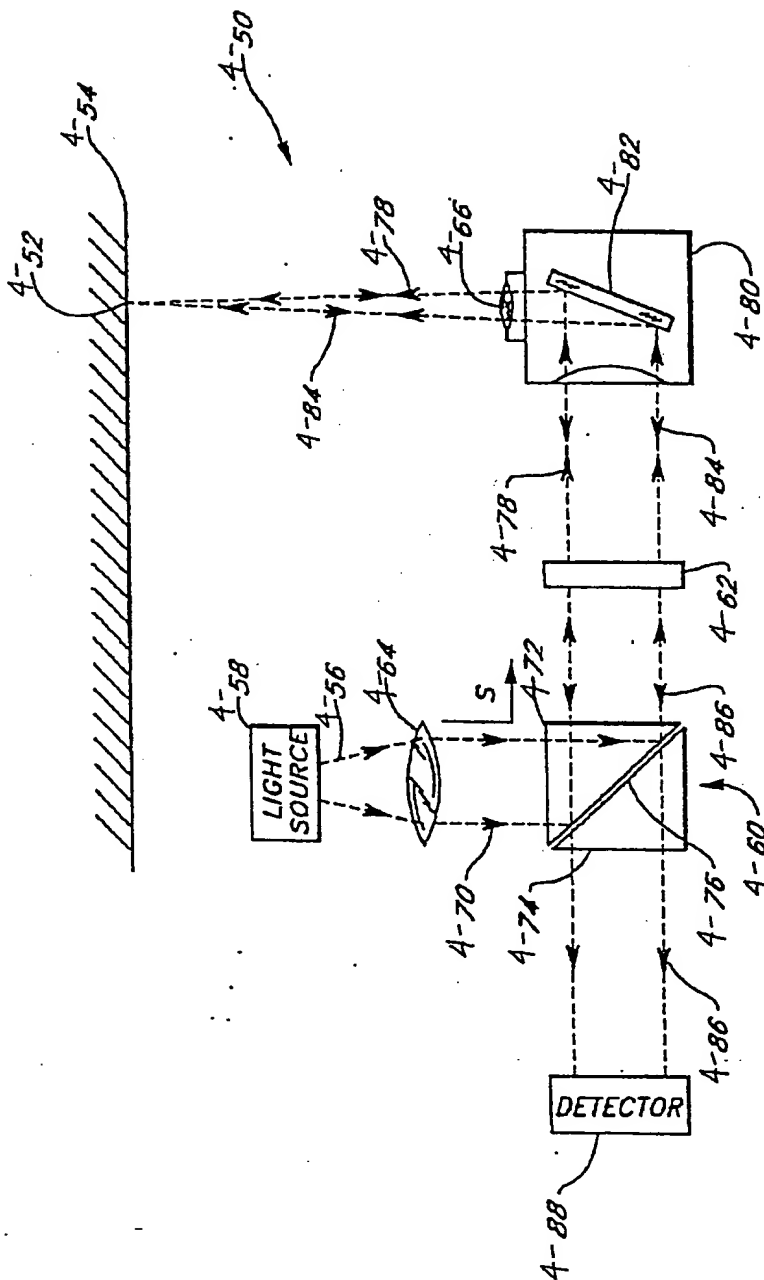
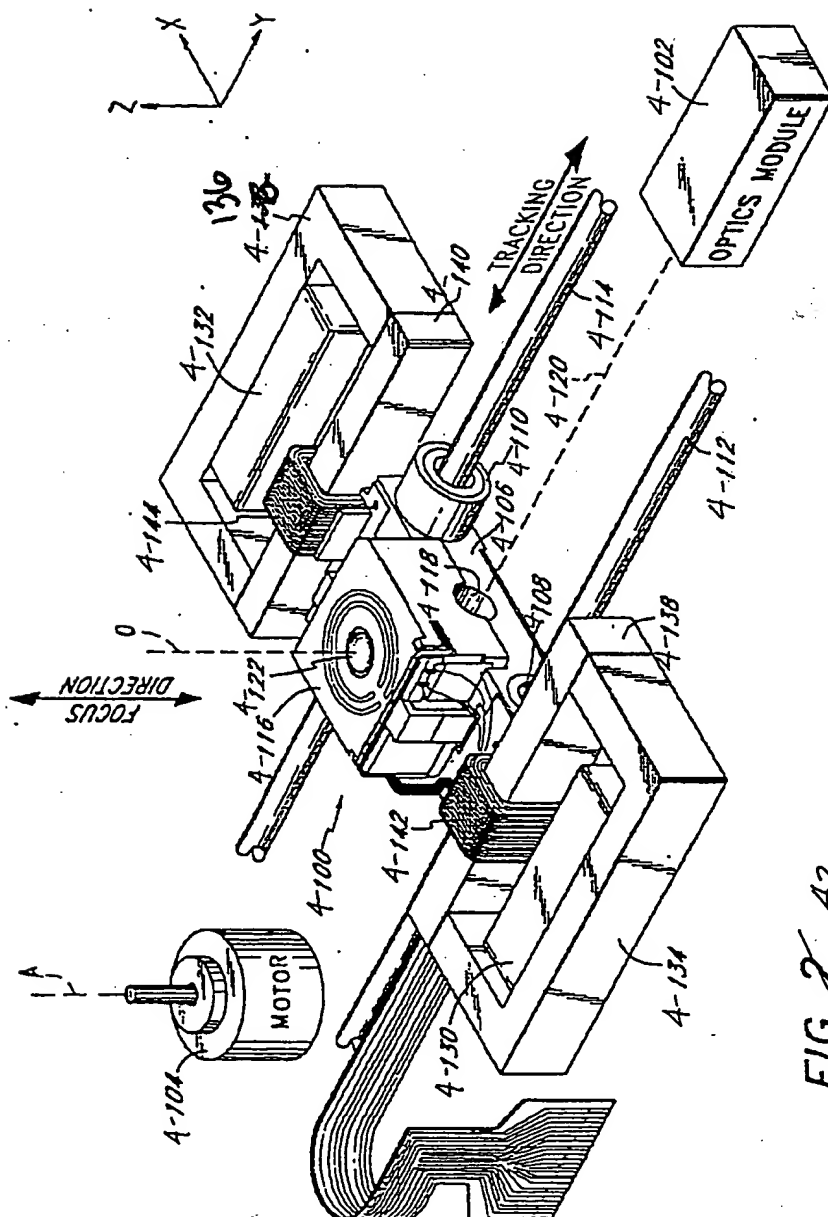


FIG. 4



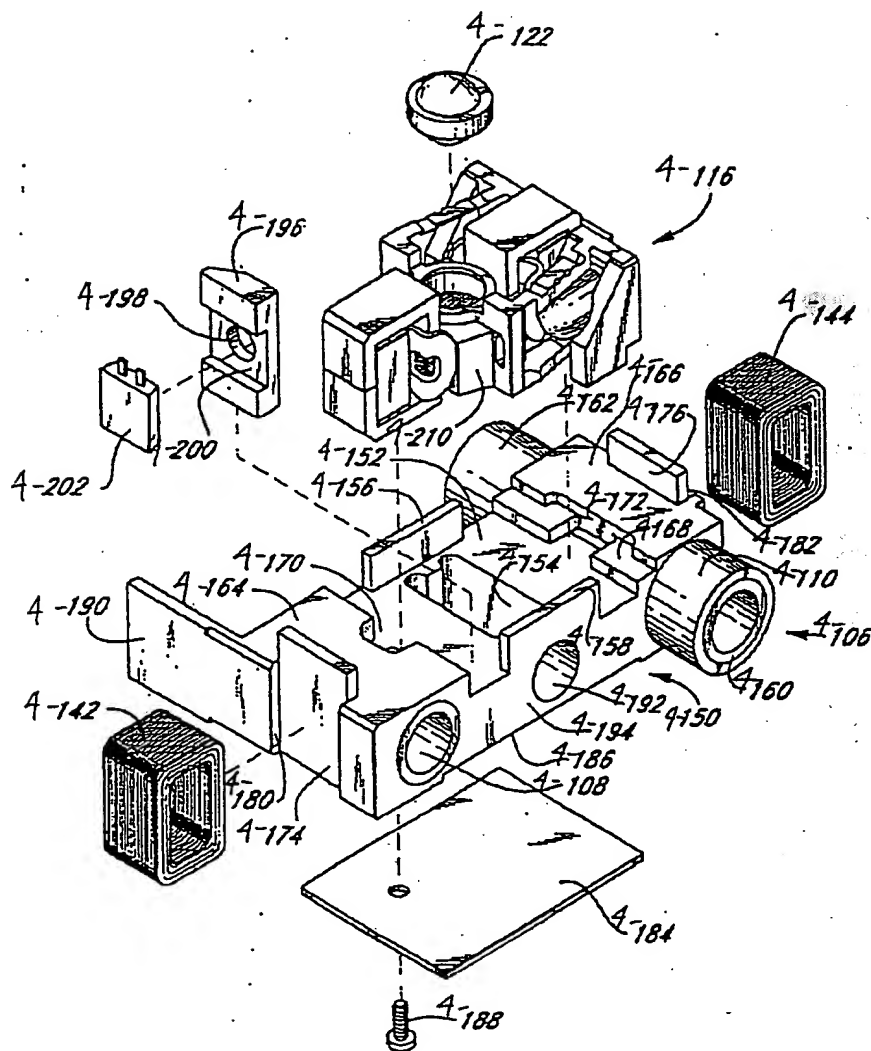


FIG. 3 43

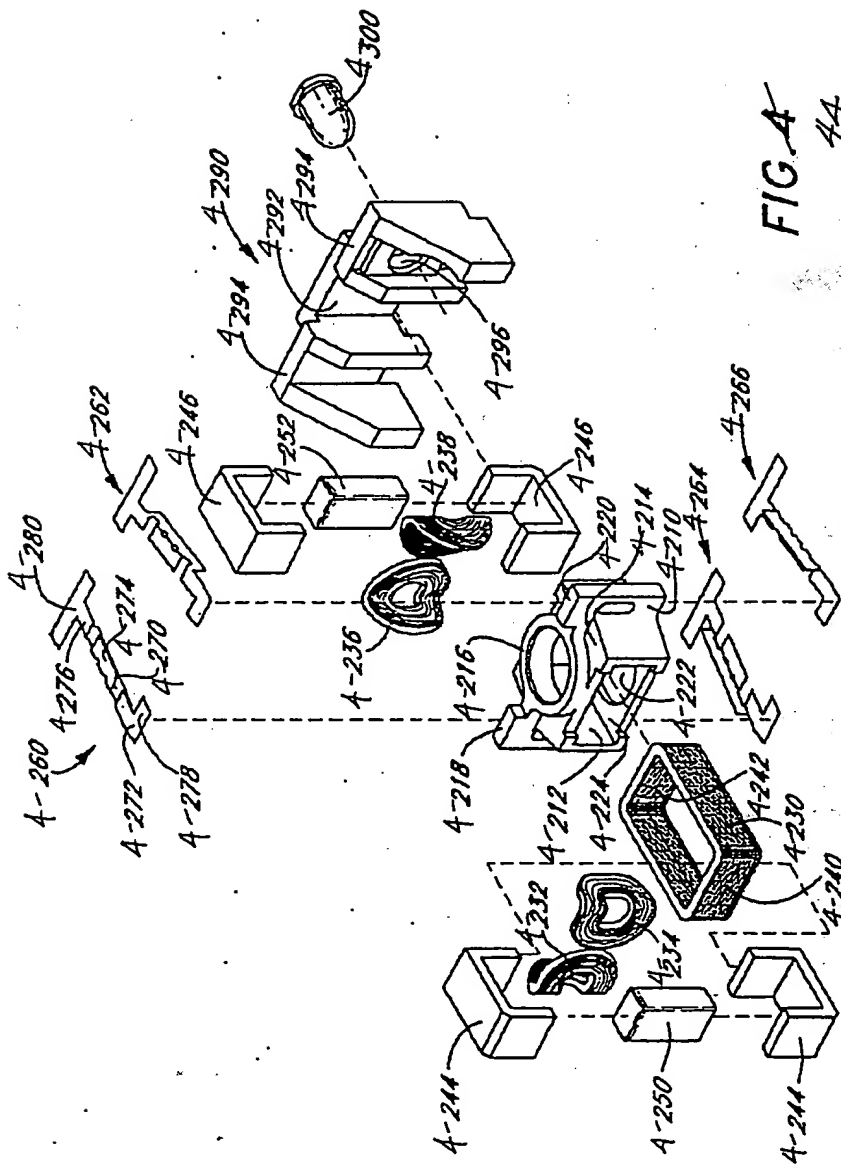


FIG. 4

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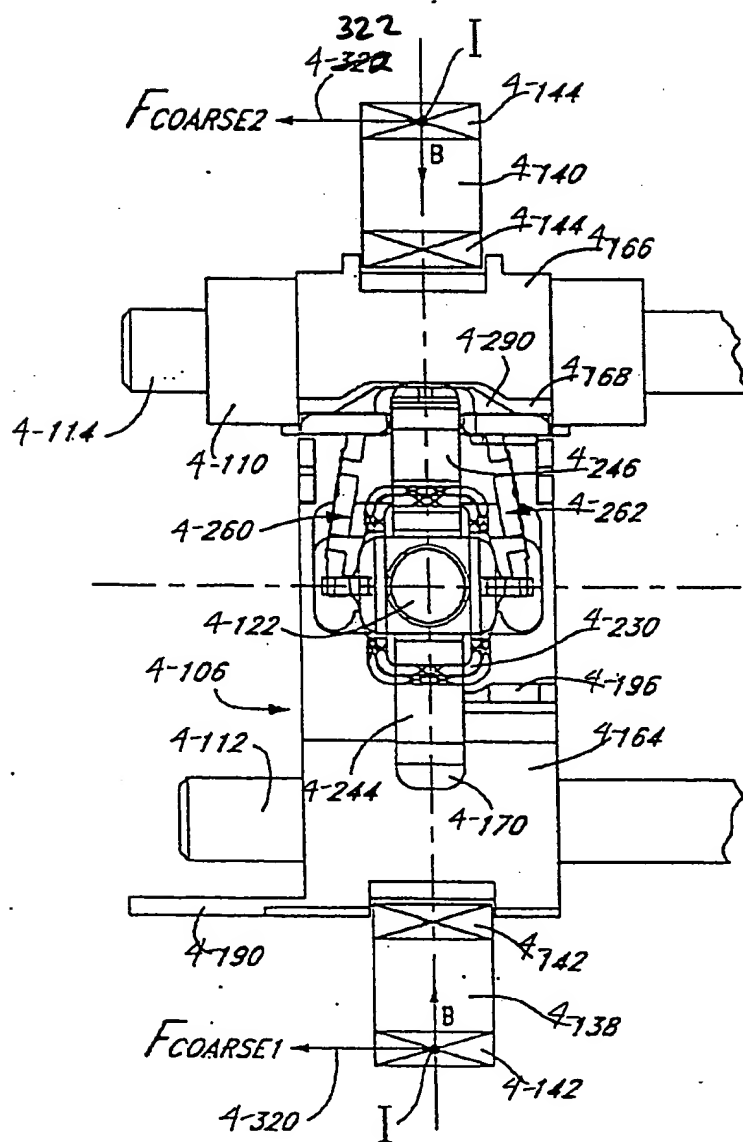


FIG. 5 45

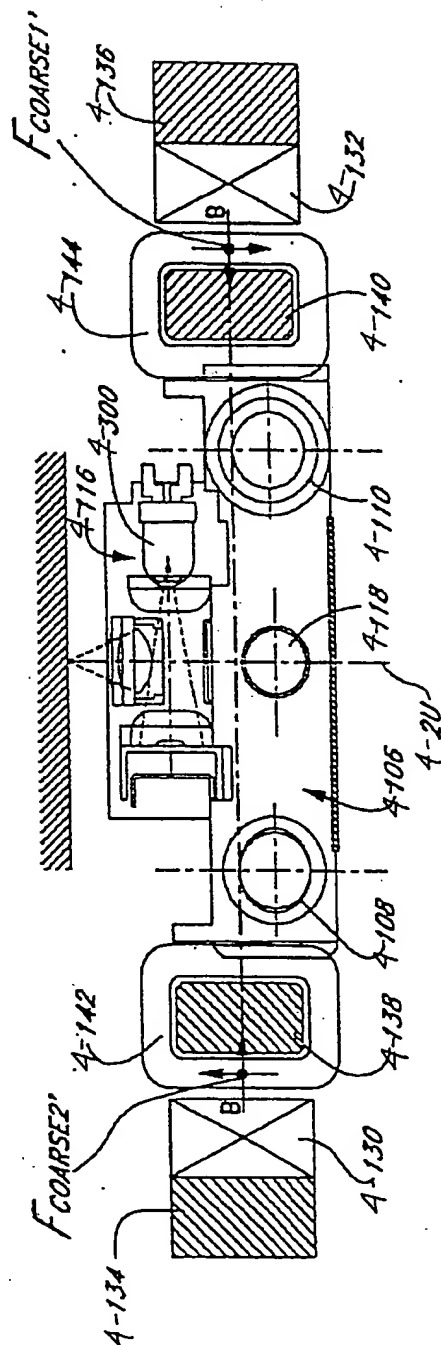


FIG. 6

36

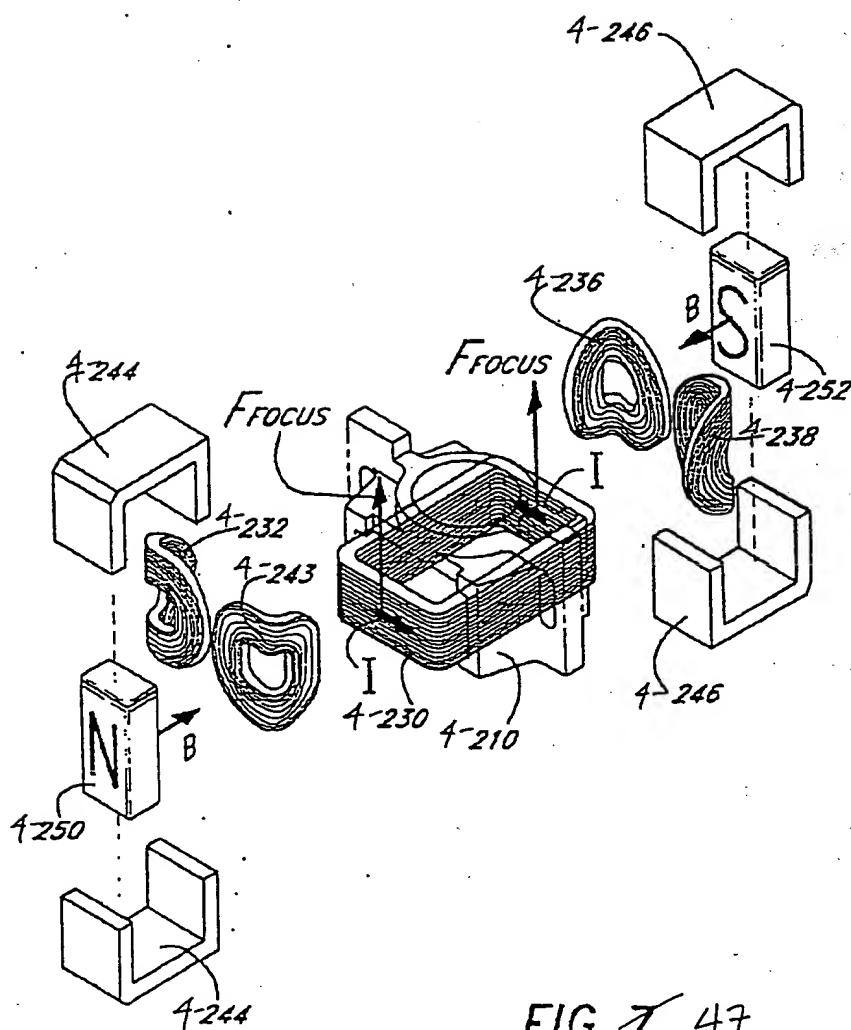


FIG. 7 47

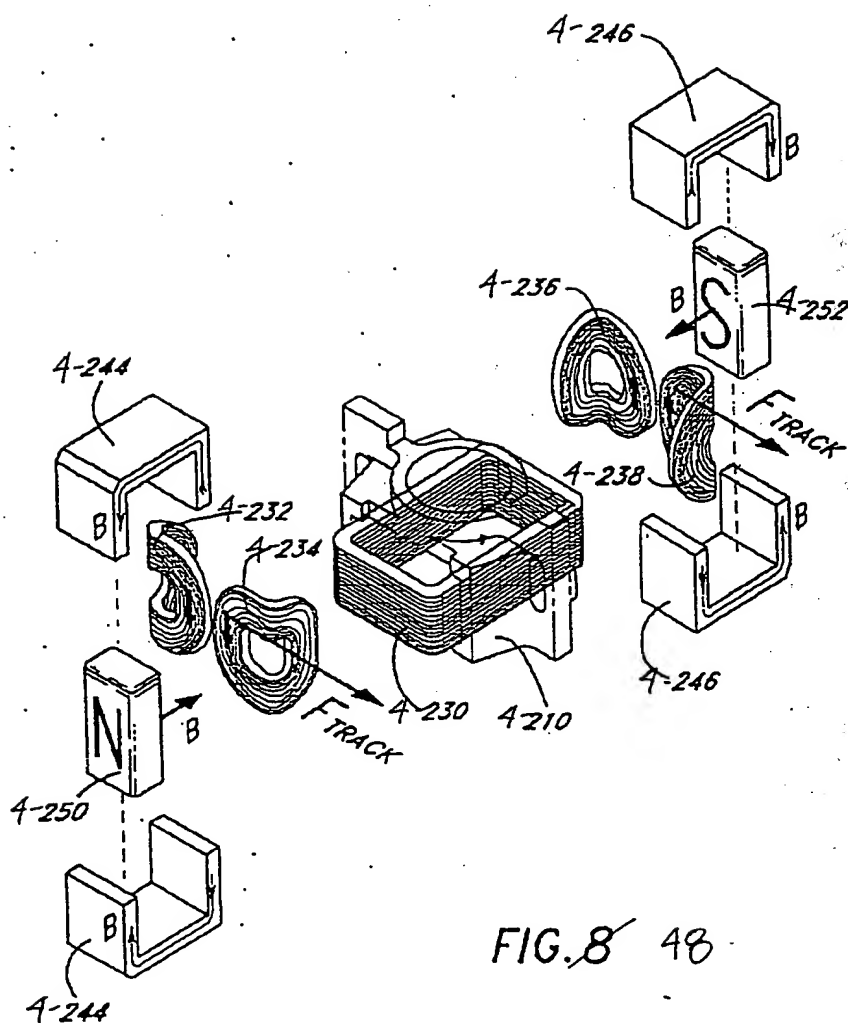


FIG. 8 48

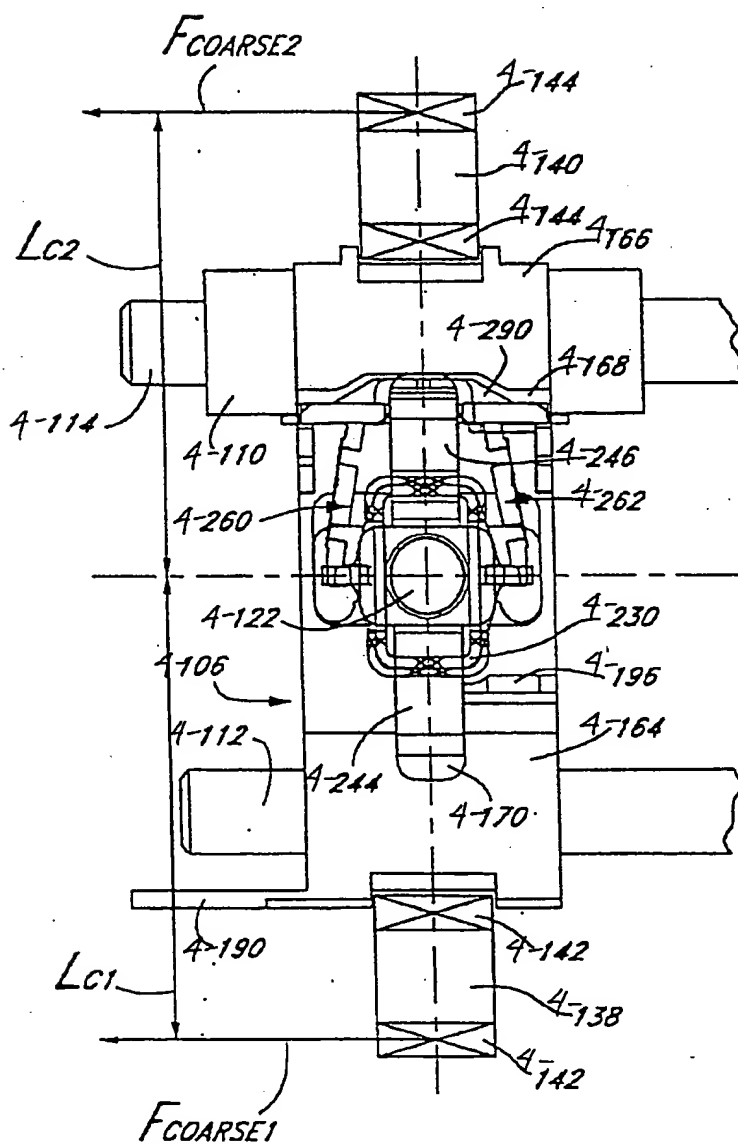
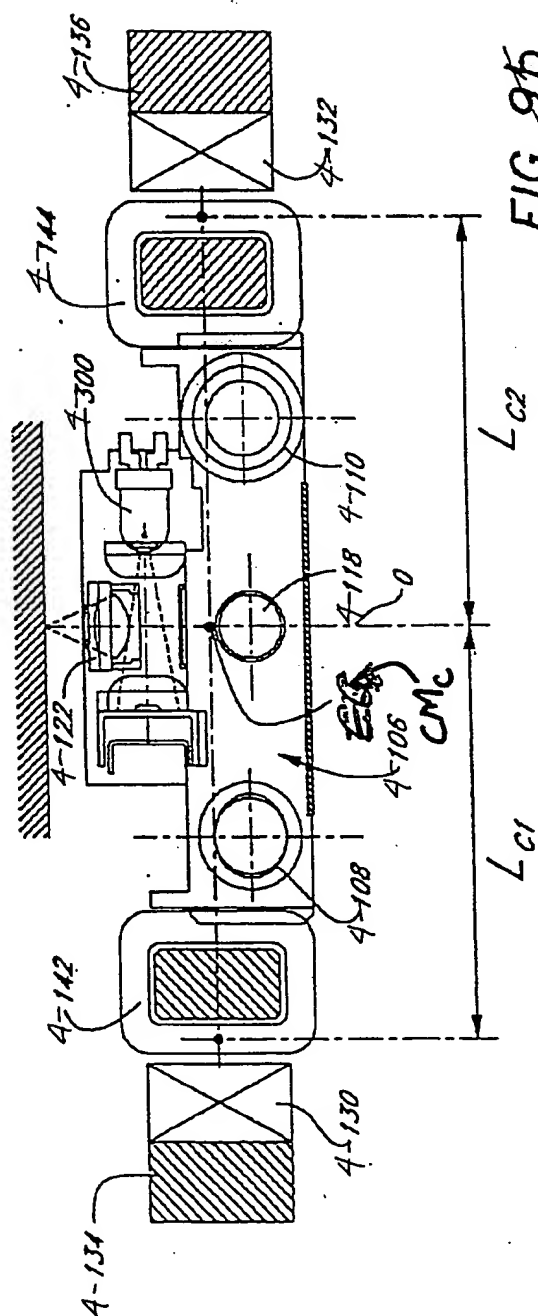


FIG. 9a
49a



496

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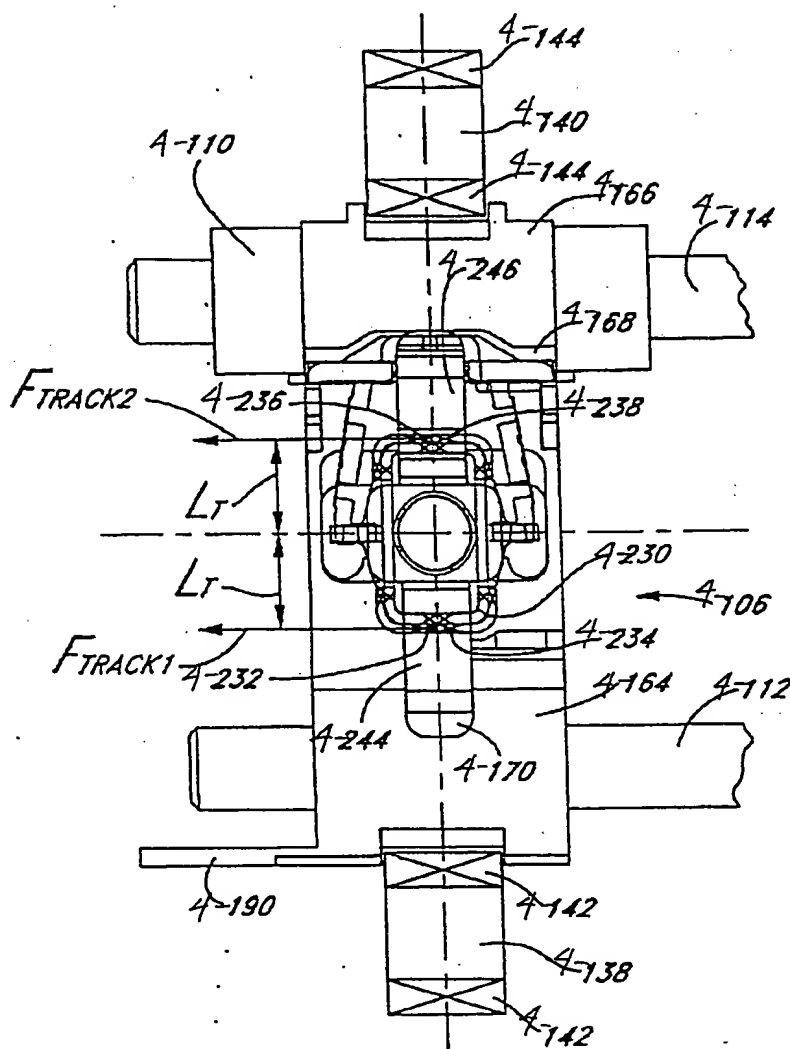
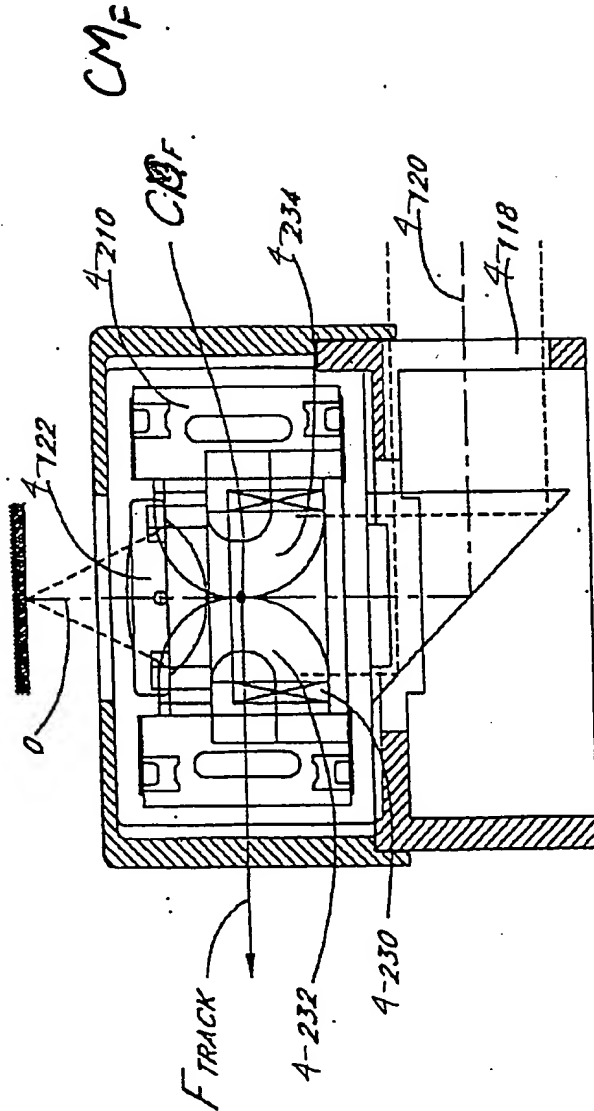


FIG. 10a
50a.

FIG. 10b
506



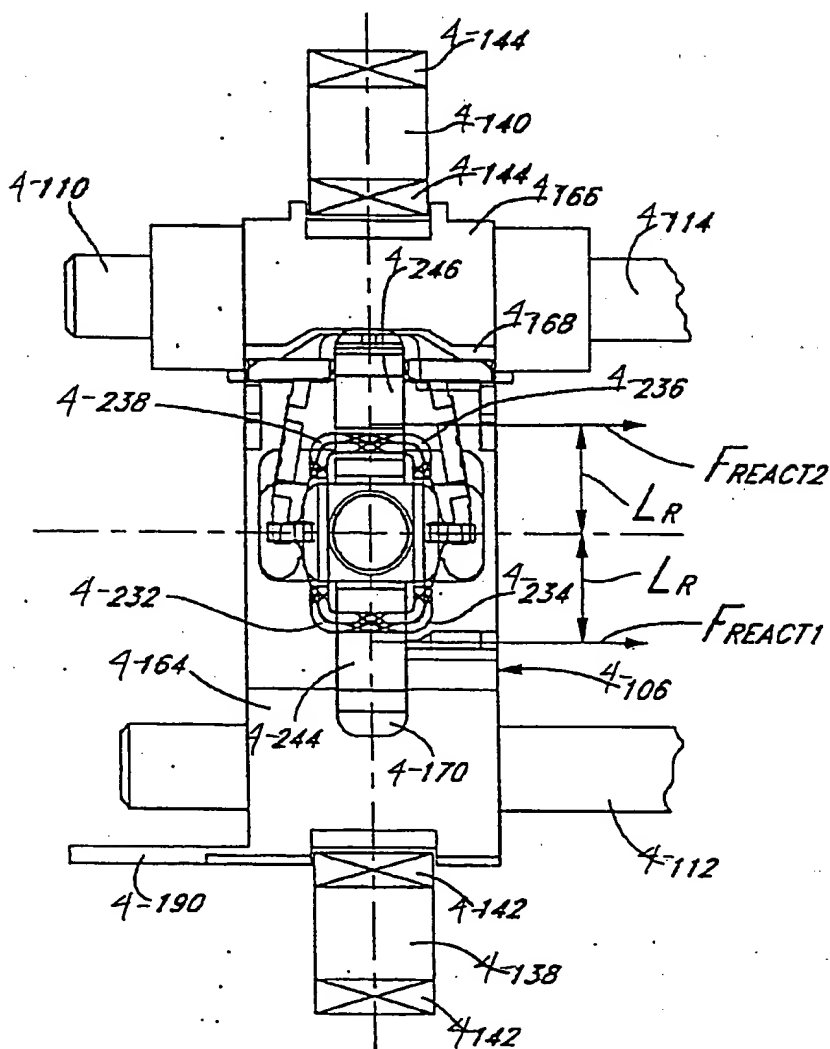


FIG. 11a

51a.

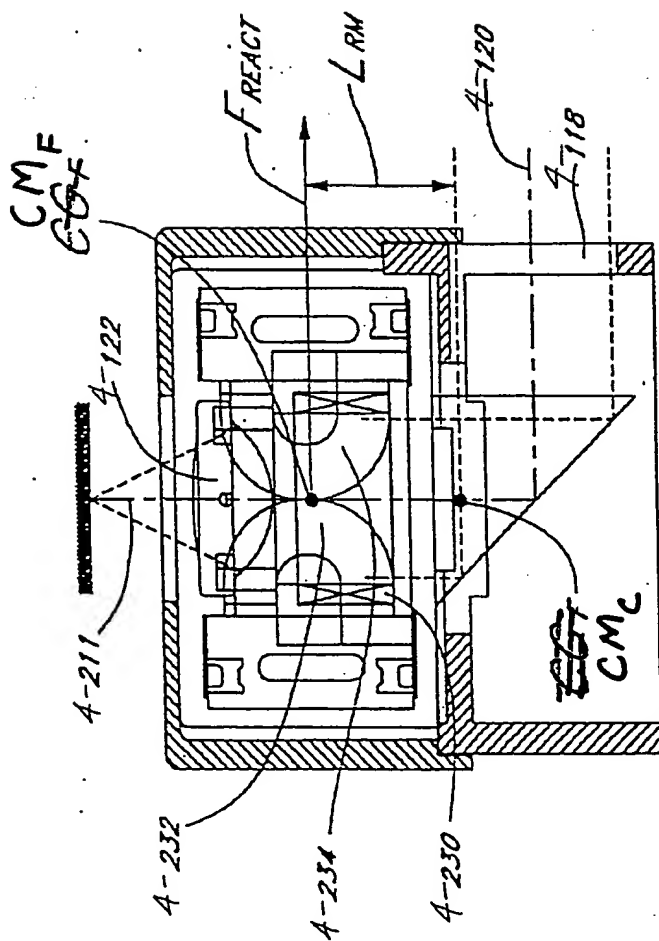


FIG. 11b
5/6

44

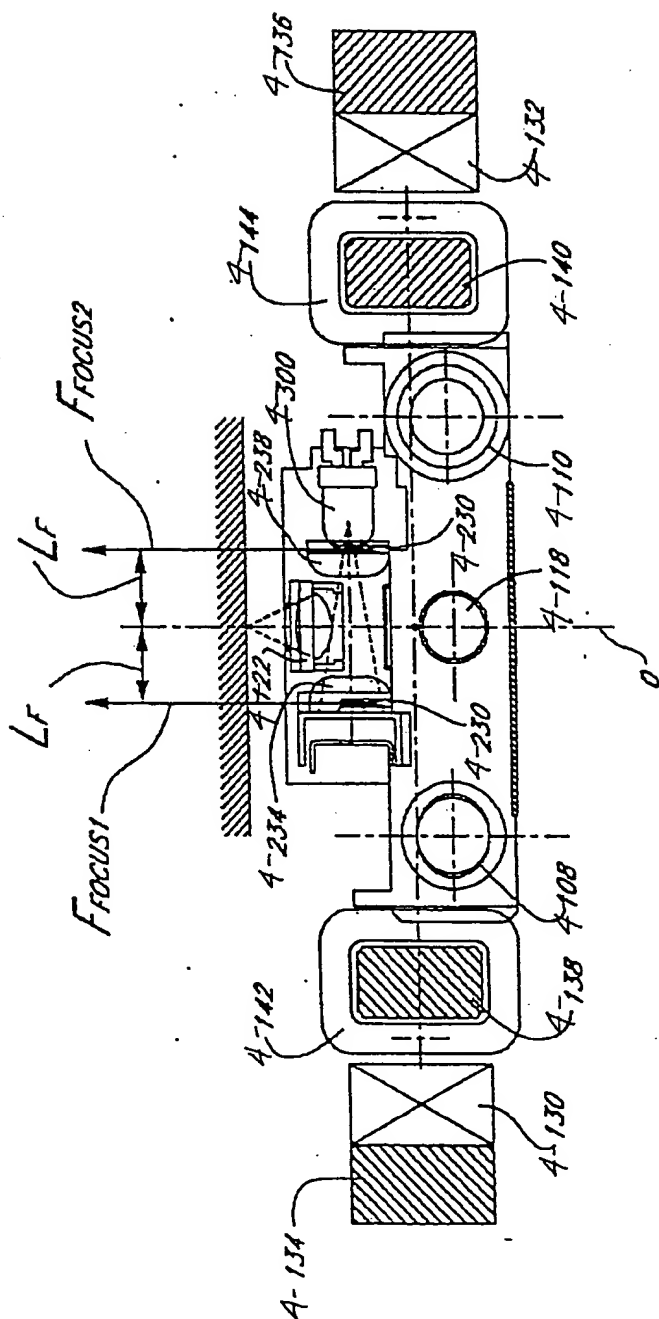
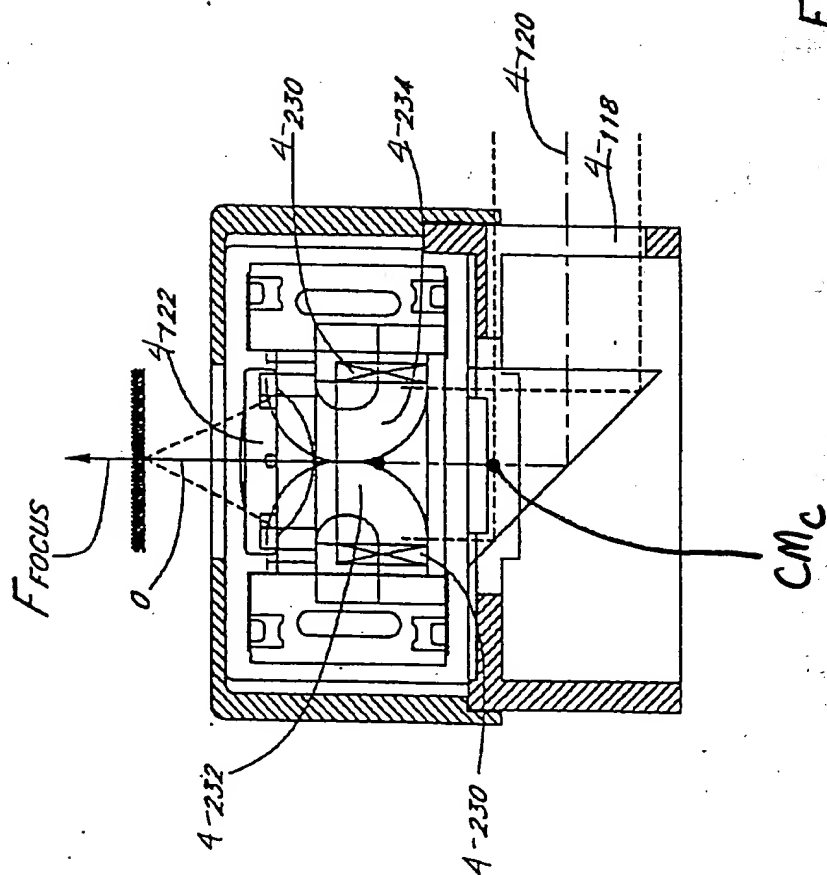


FIG. 12a
52a

45



46

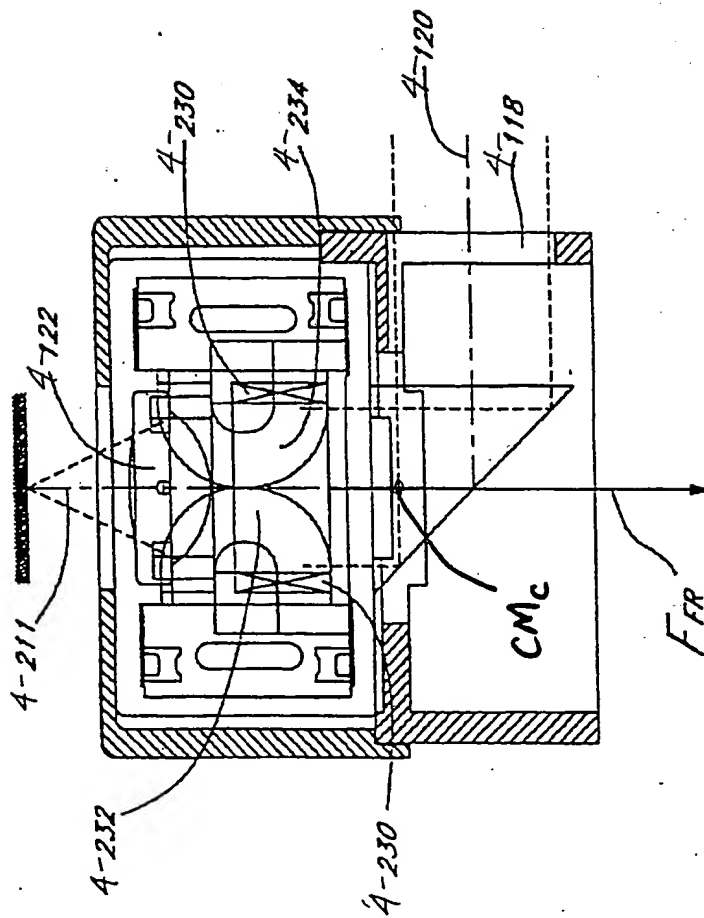


FIG. 13b
53b

49

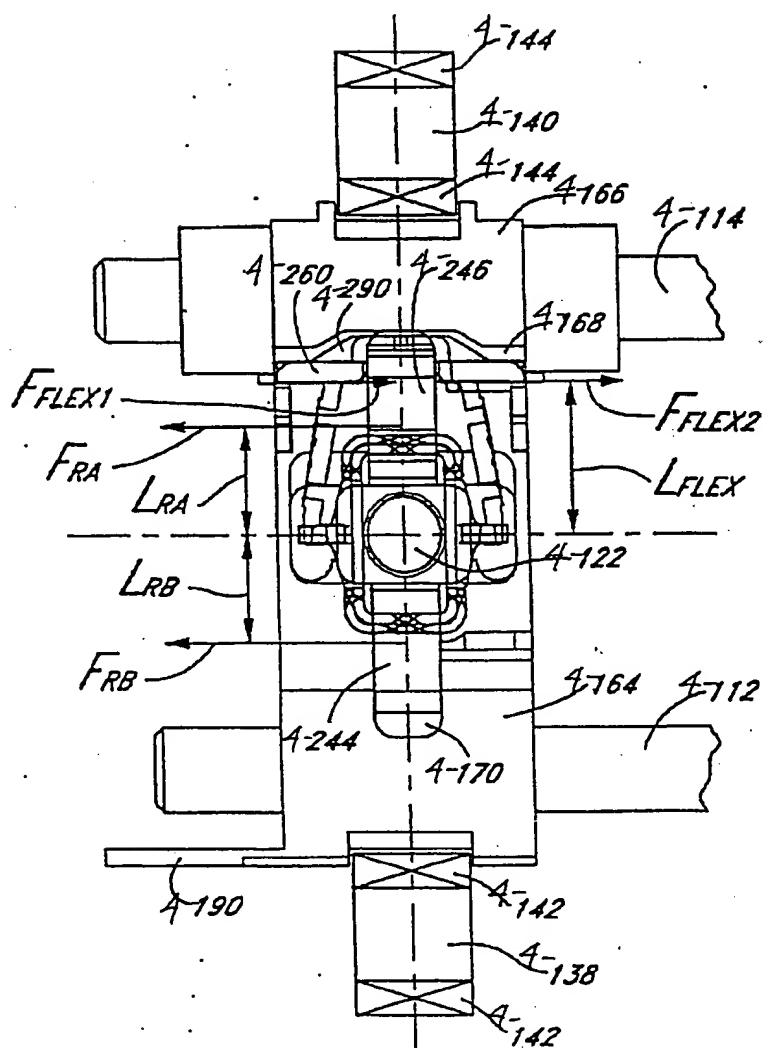


FIG. 1A 54

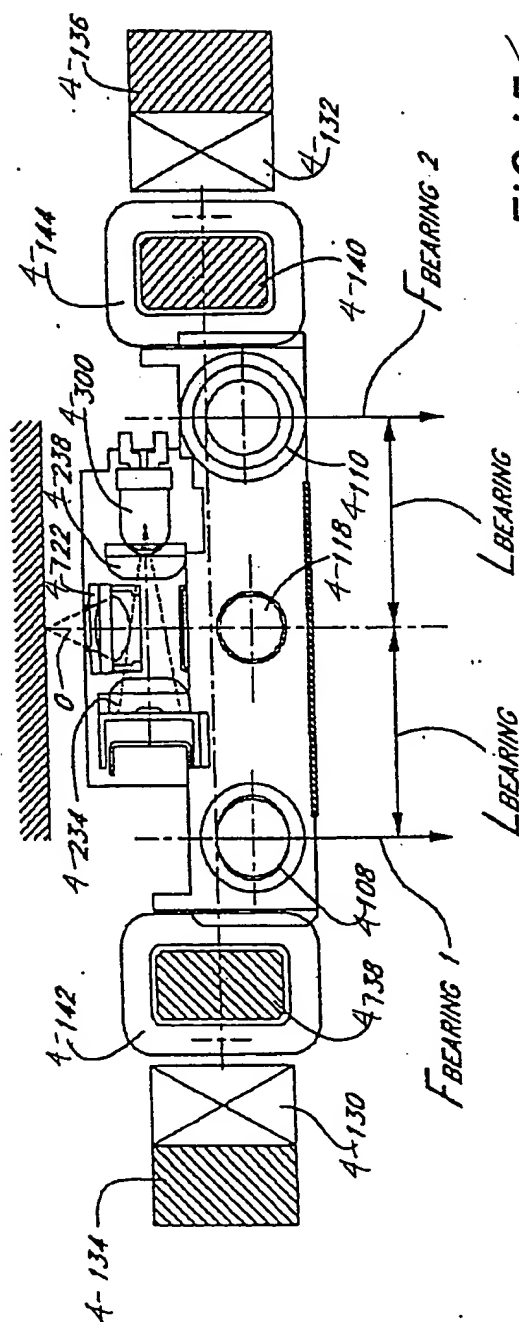


FIG. 15a
55a

50

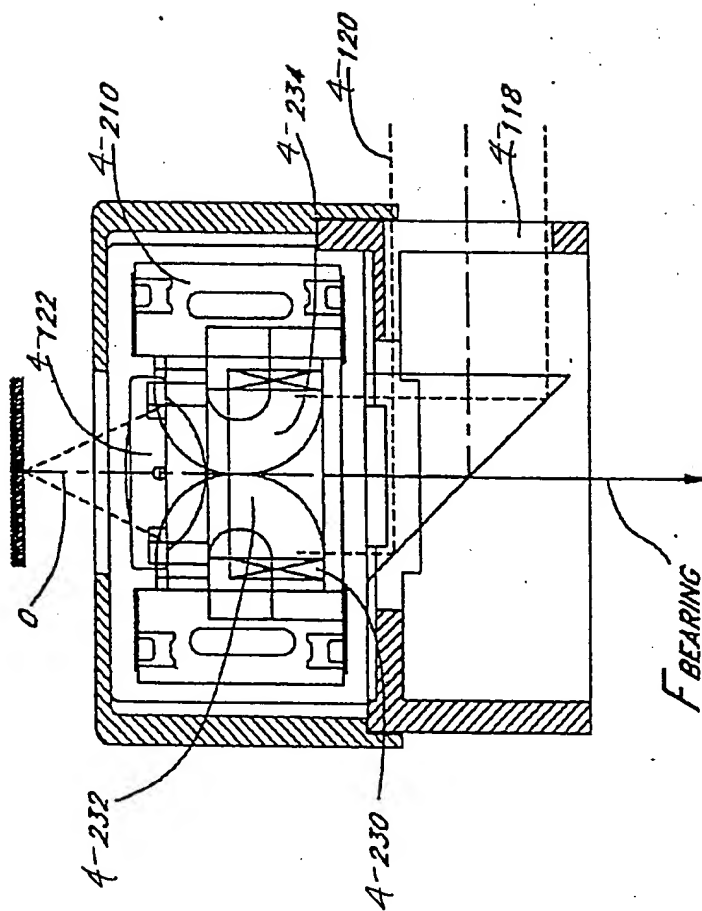


FIG. 15b
55b

51

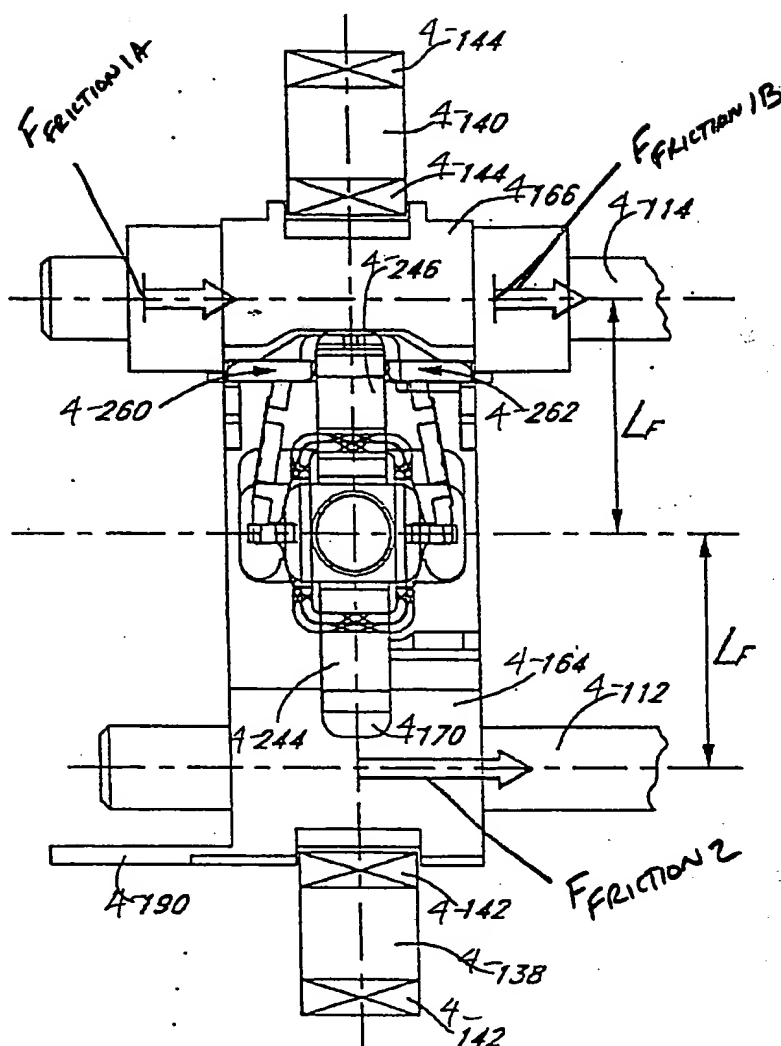


FIG. 16a
56a

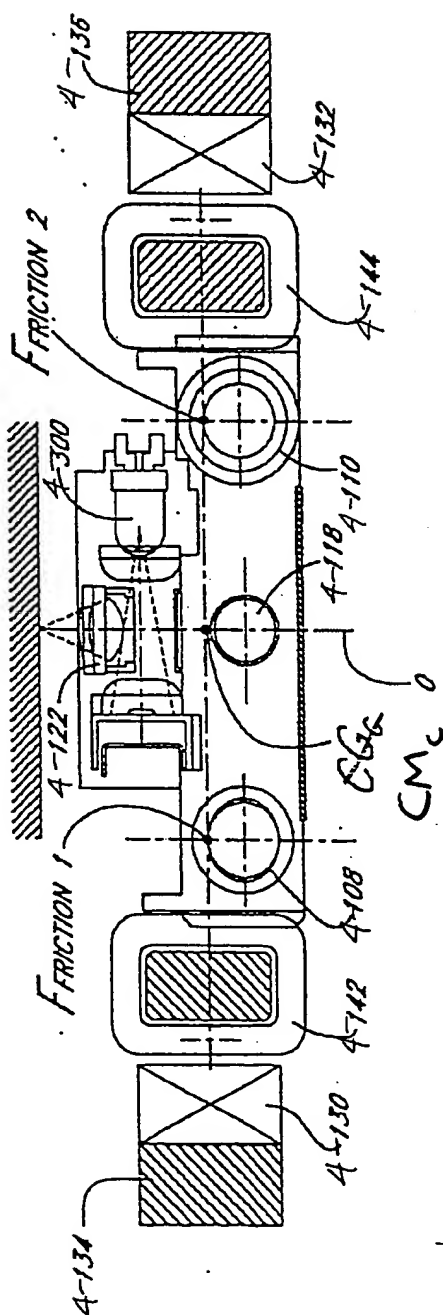


FIG. 16b
566.

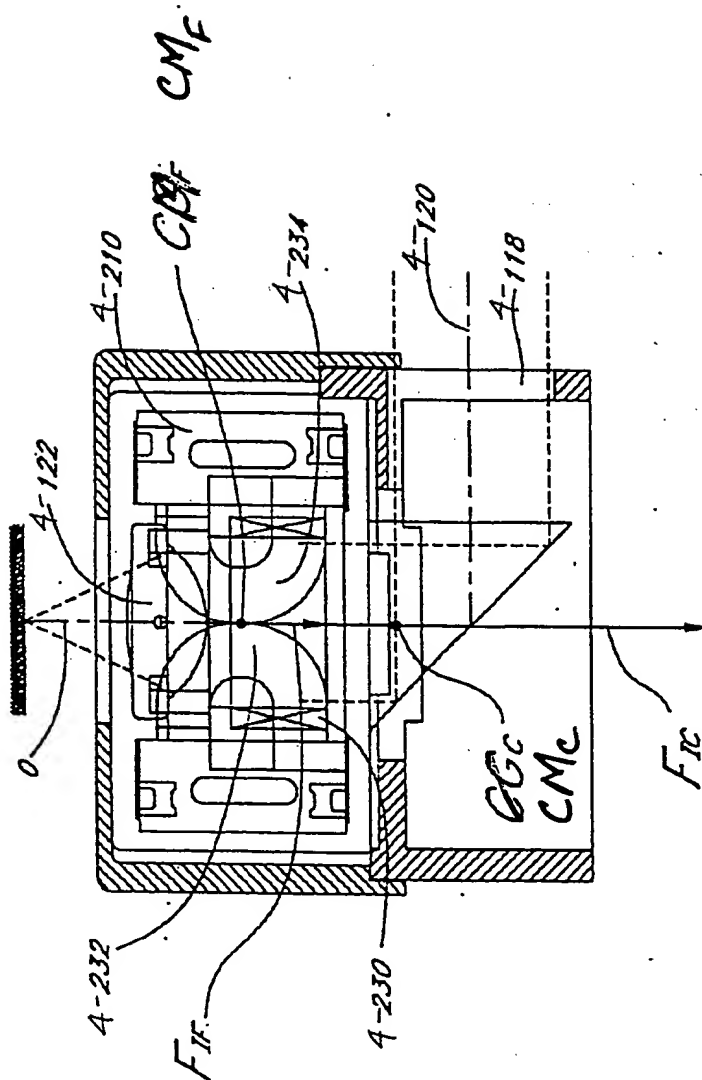
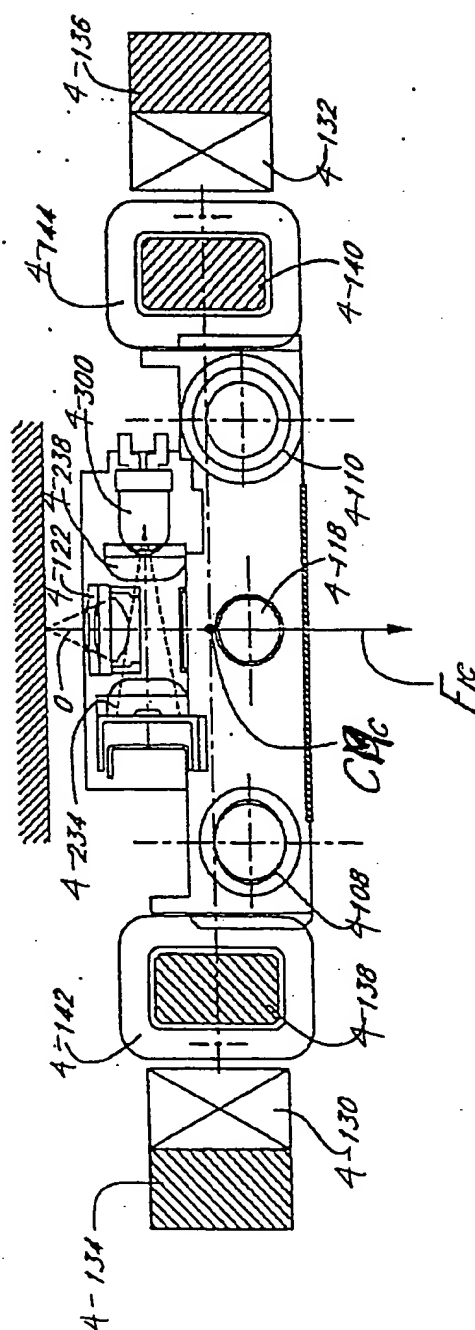


FIG. 17 S7

54



586

56

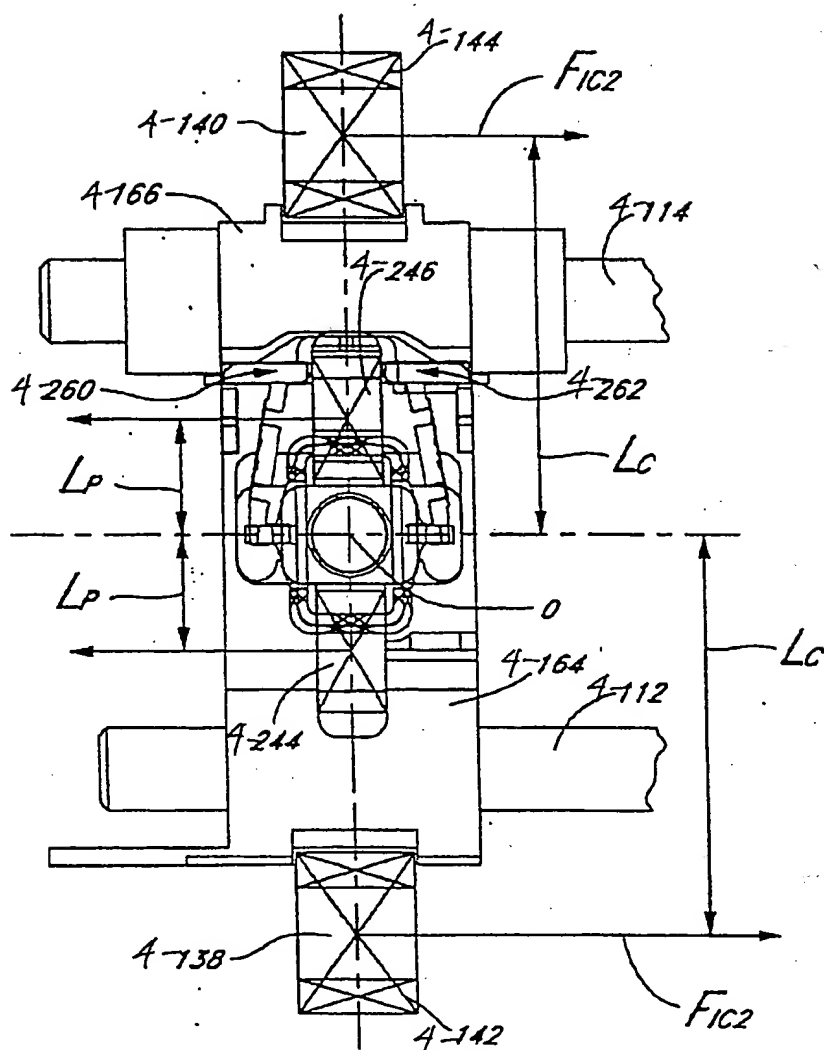


FIG. 19a
59a

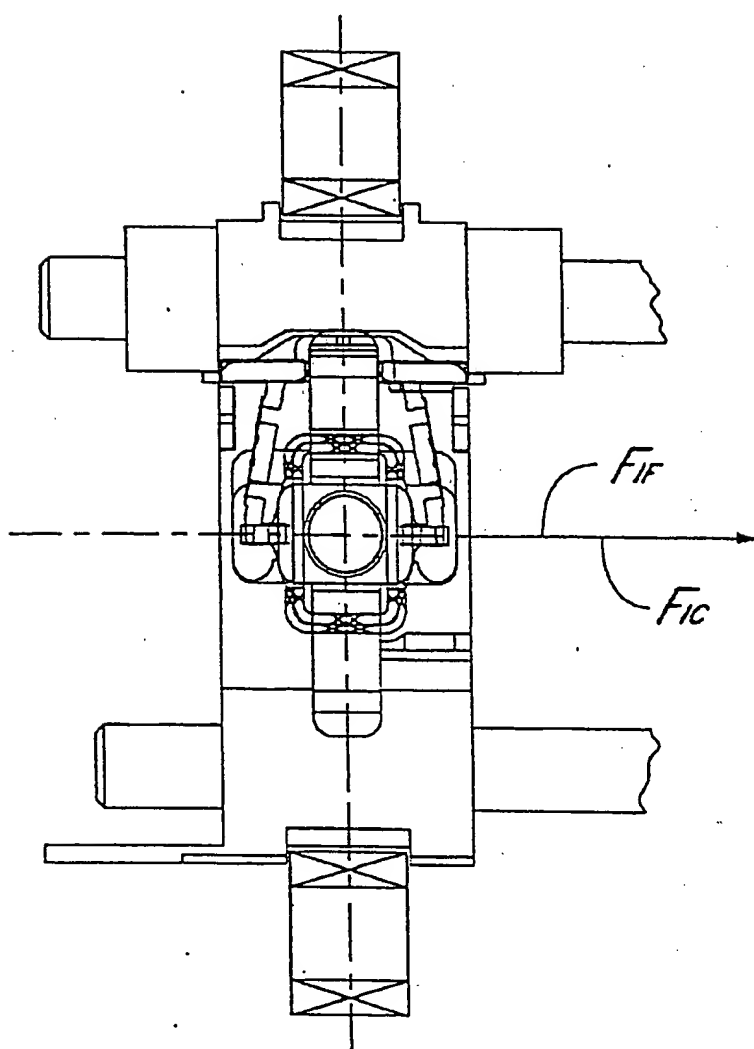


FIG. 19b
59b.

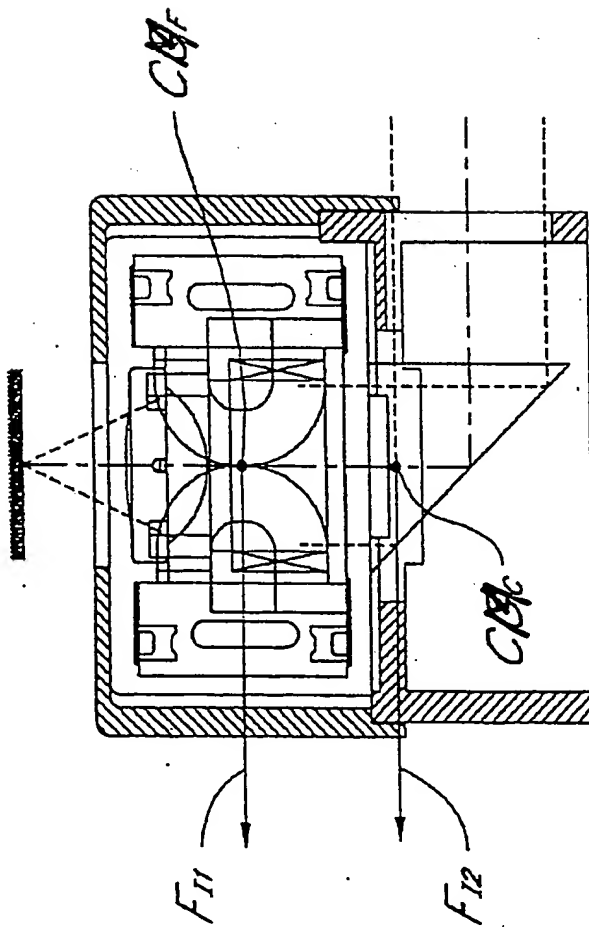
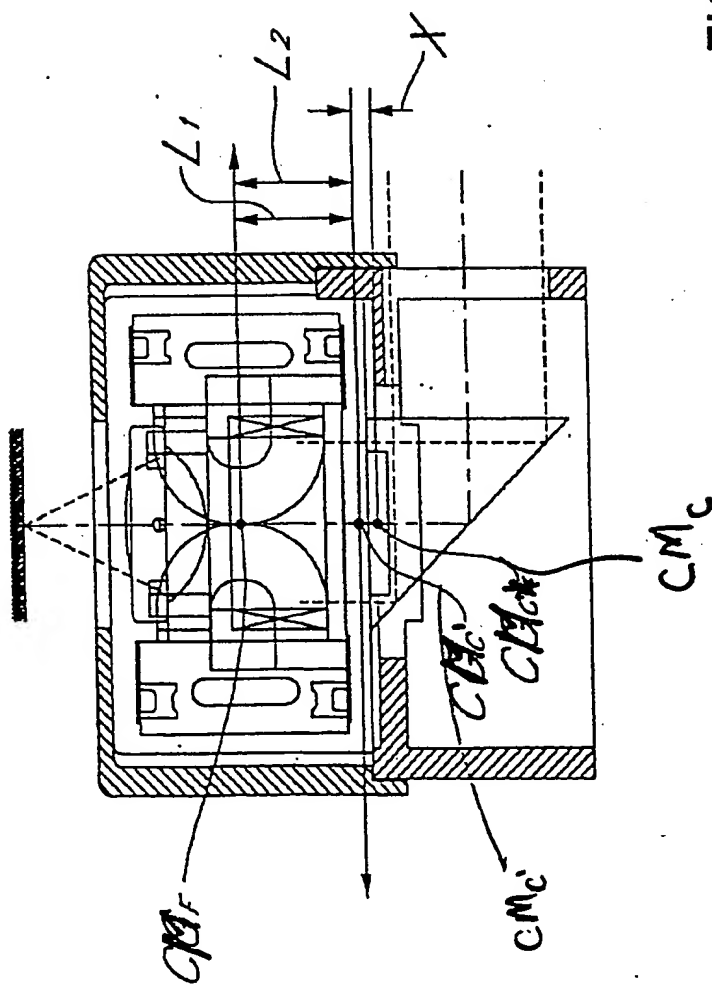


FIG. 20a
60a.

59



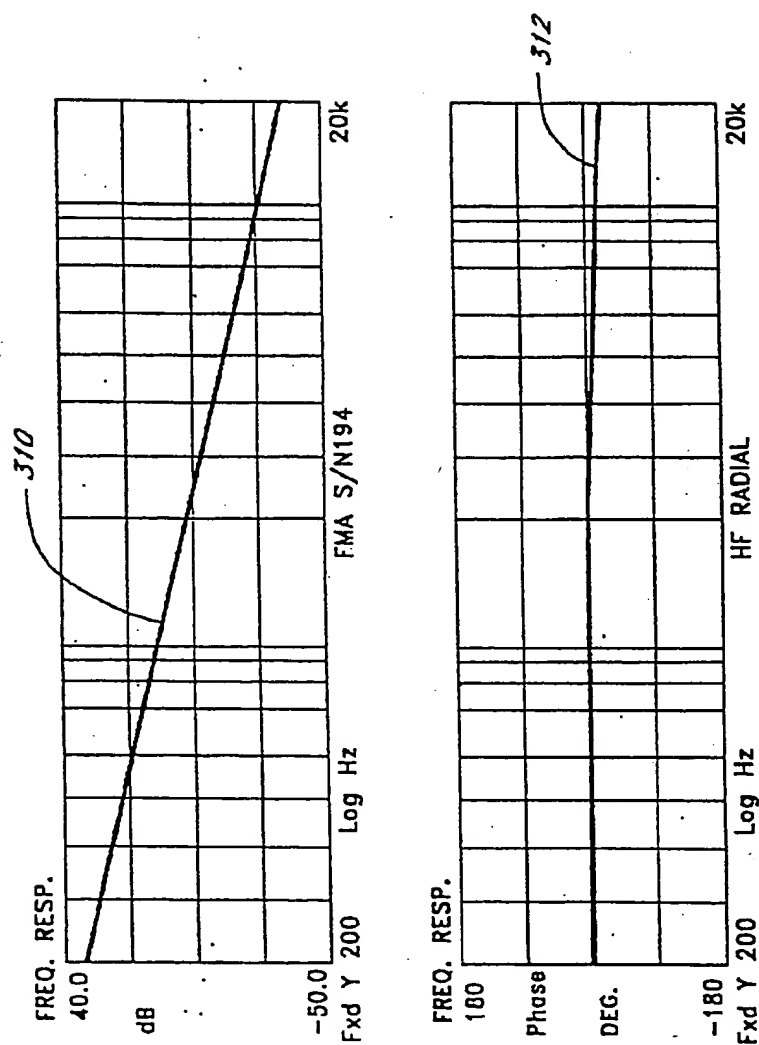


FIG. 210
61a

61

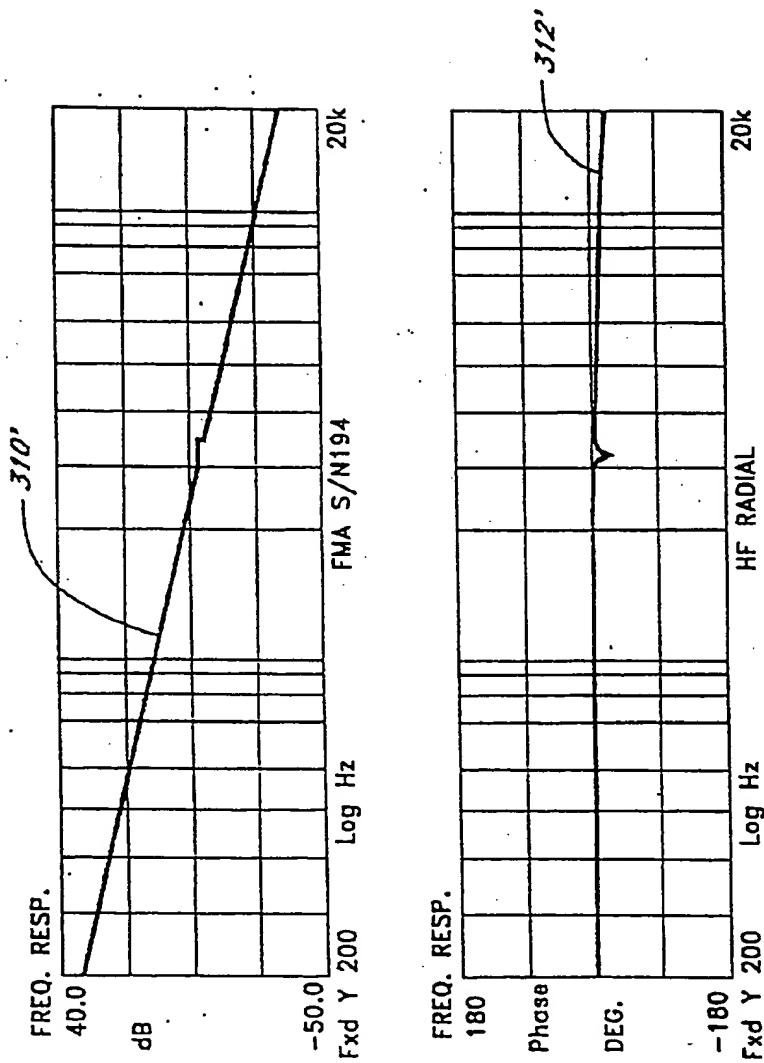


FIG. 21b
616

62

FIG. 22a
62a

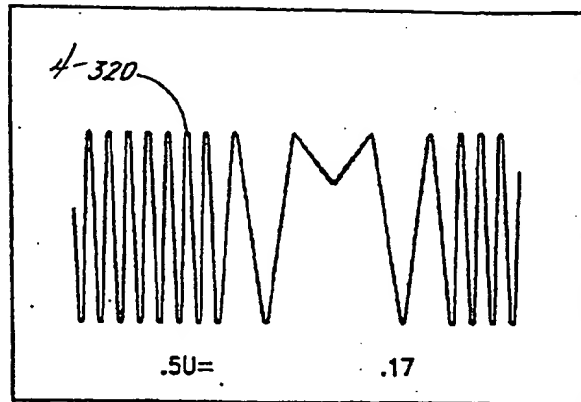


FIG. 22b
62b

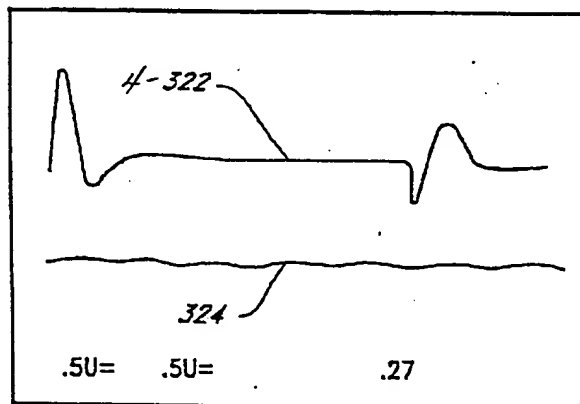
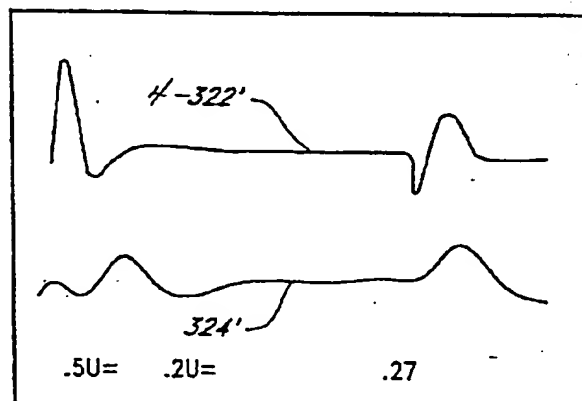


FIG. 22c
62c



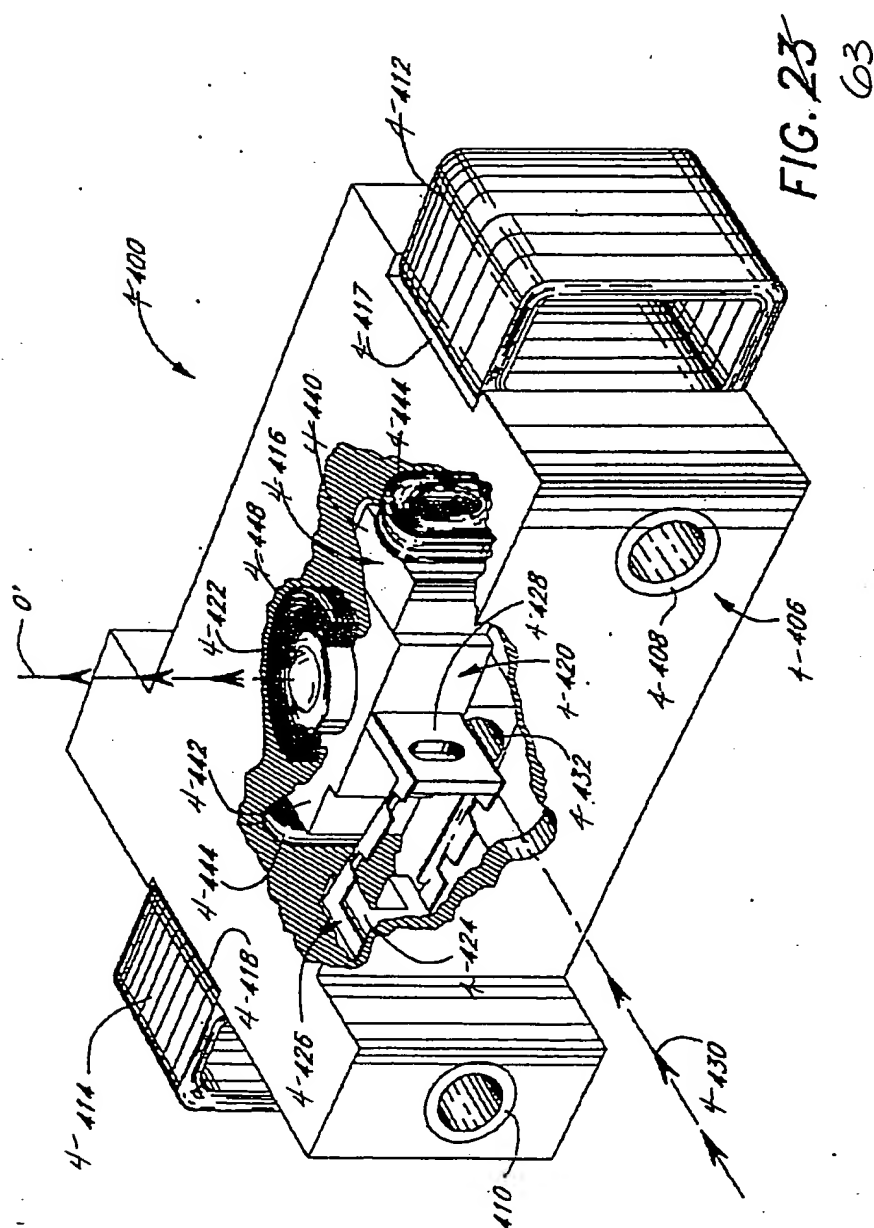


FIG. 24 64

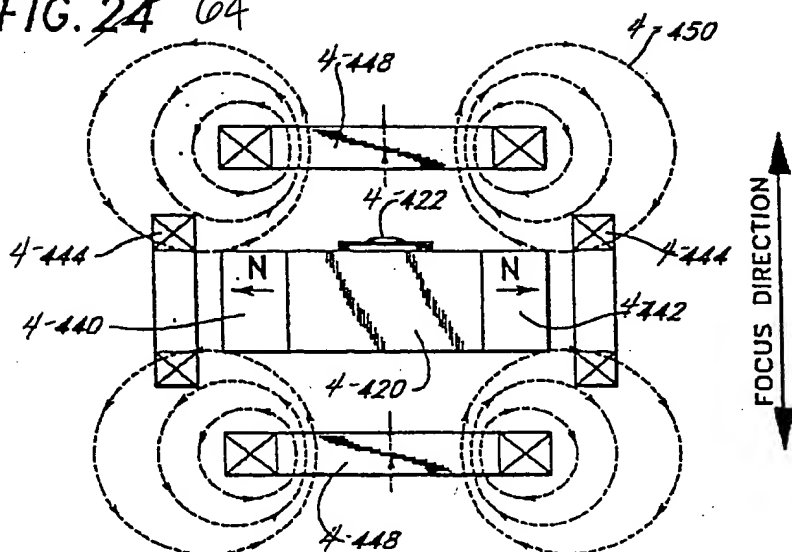
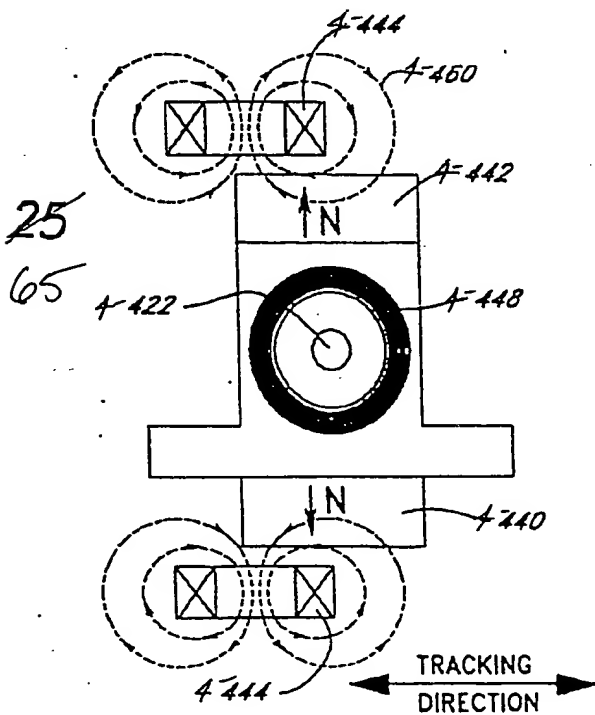
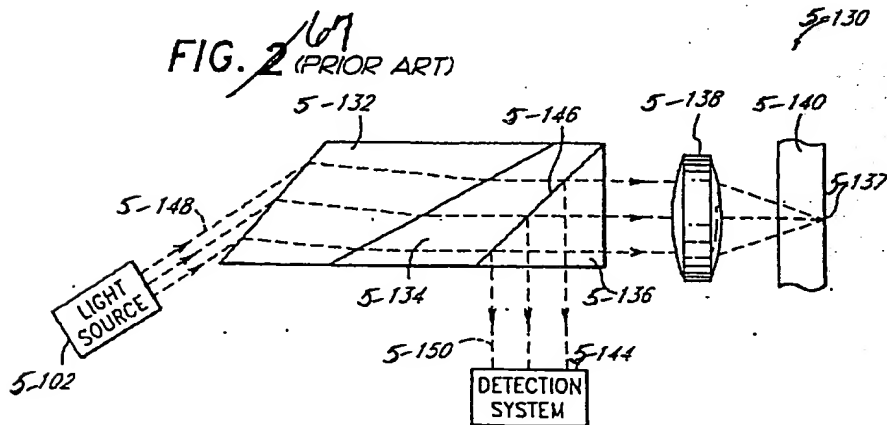
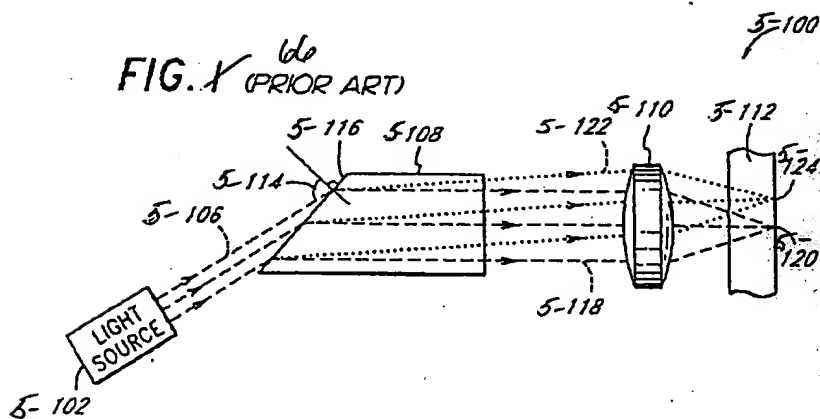
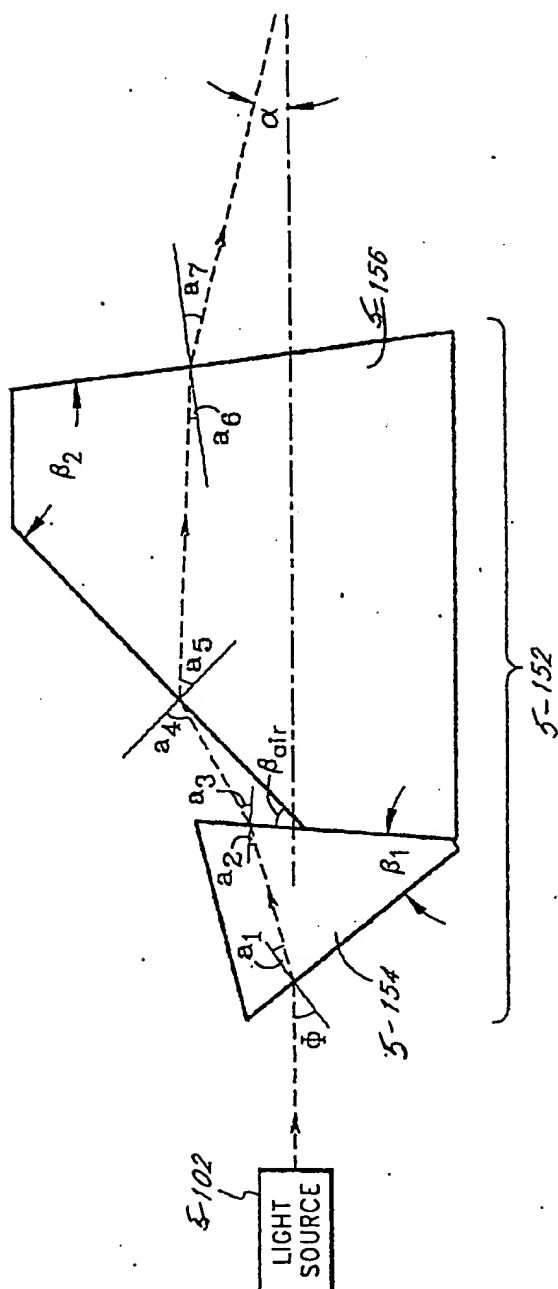


FIG. 25 65







69

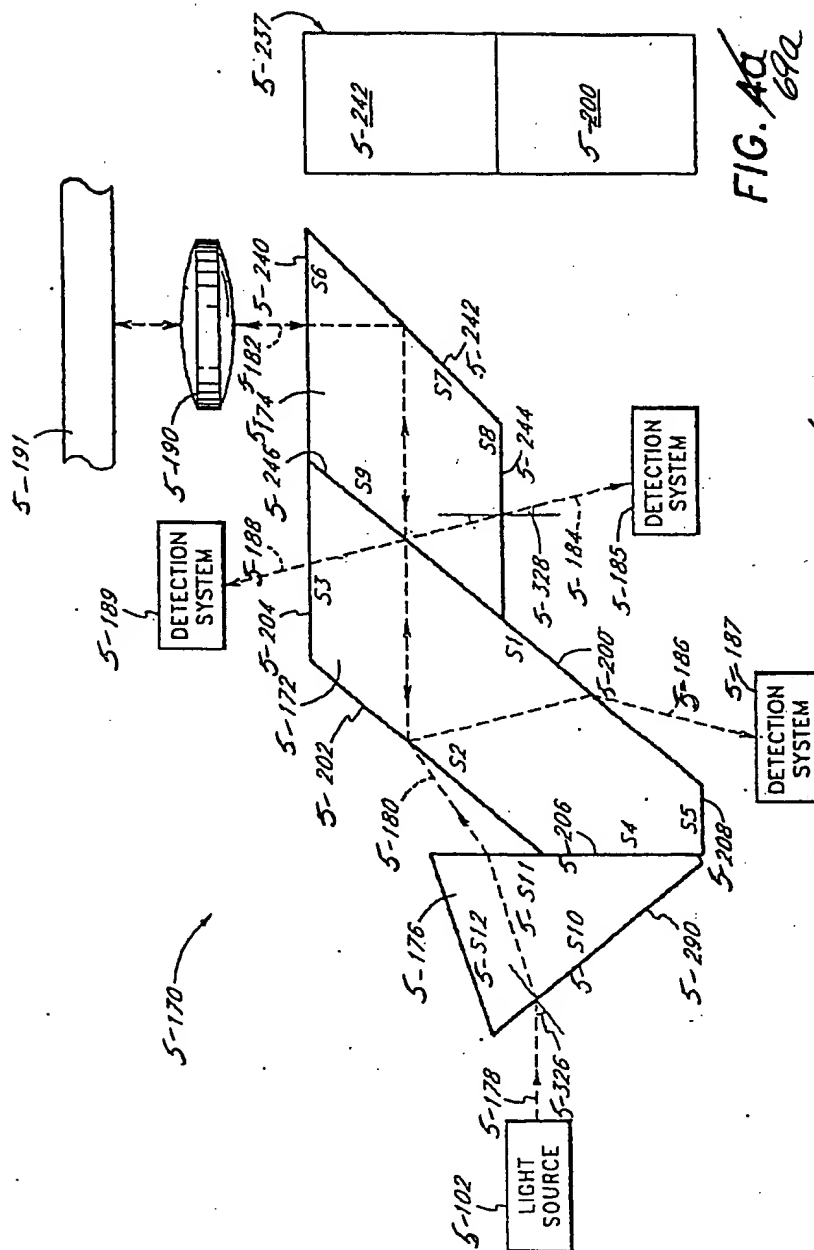


FIG. 169

FIG. 169a

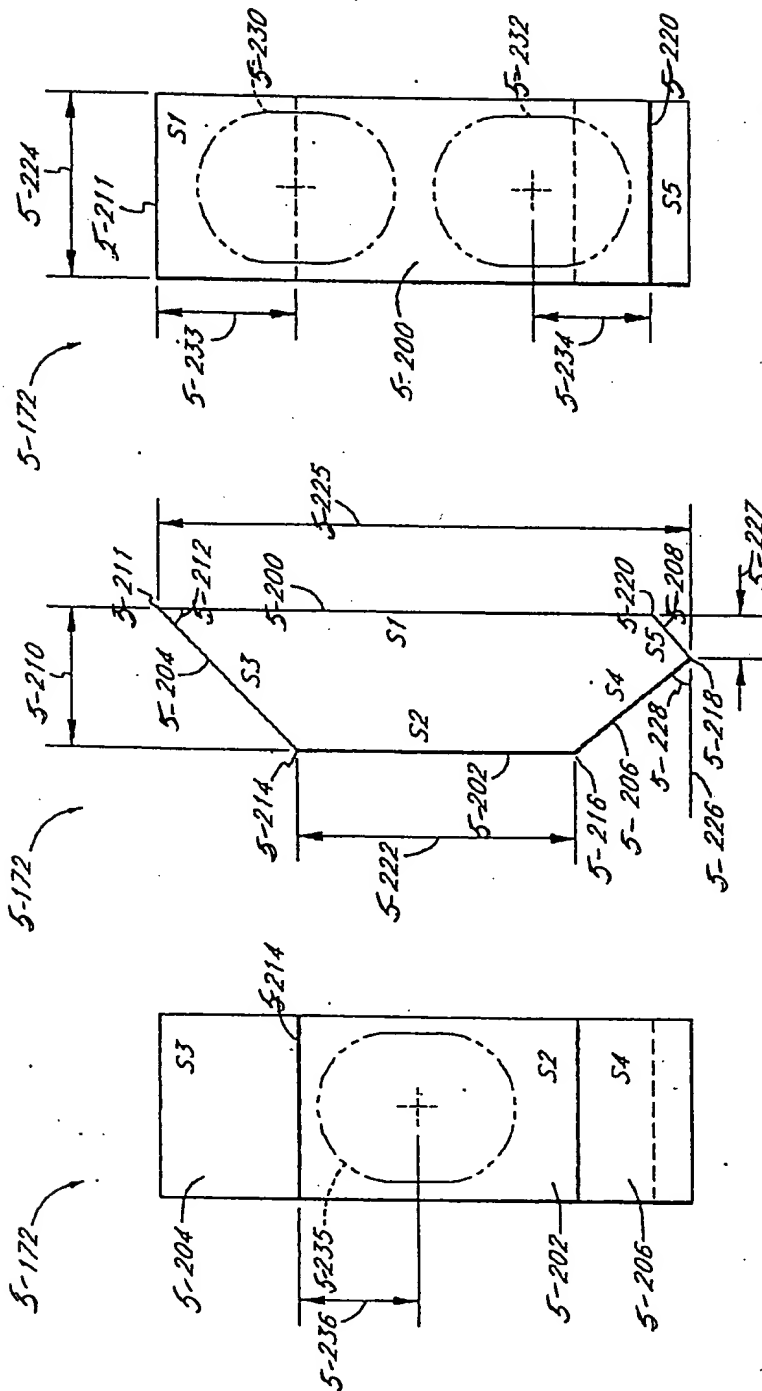
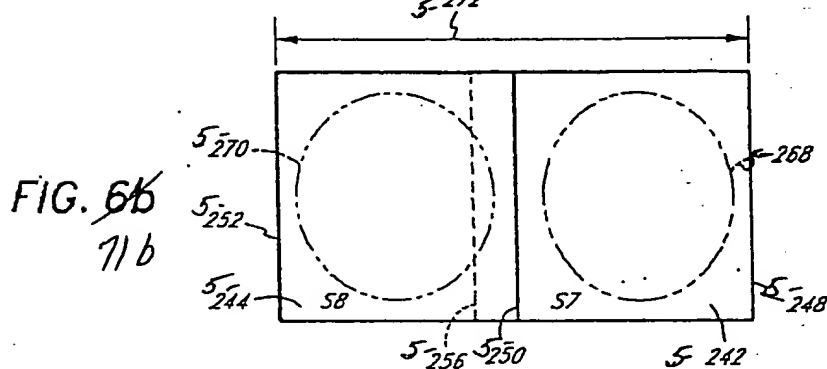
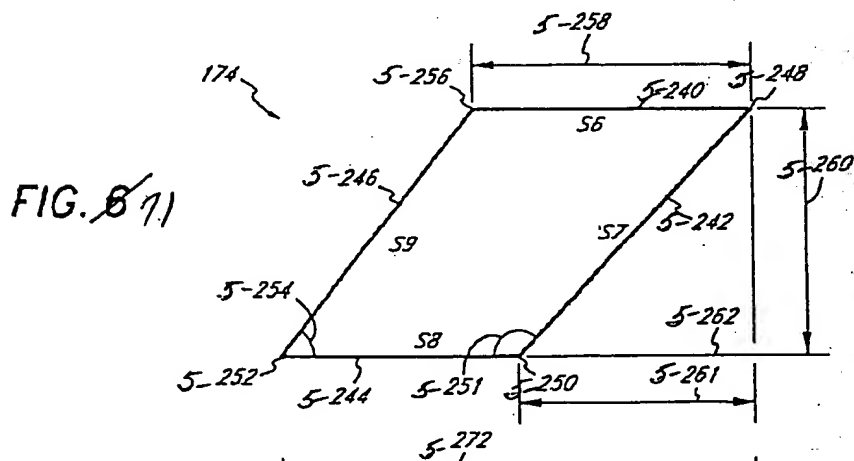
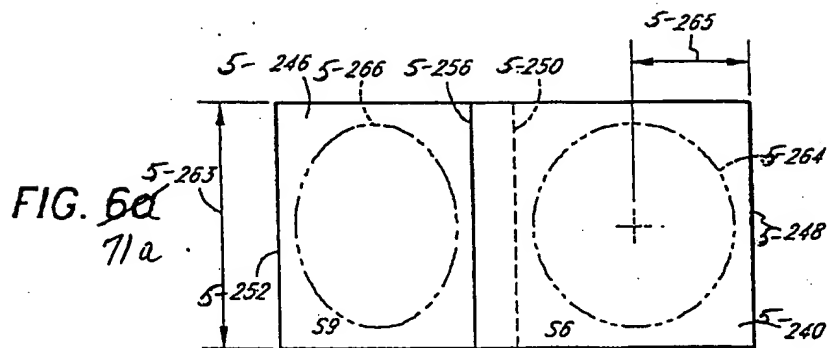


FIG. 5a
70a

FIG. 5b
70b

FIG. 5c
70c



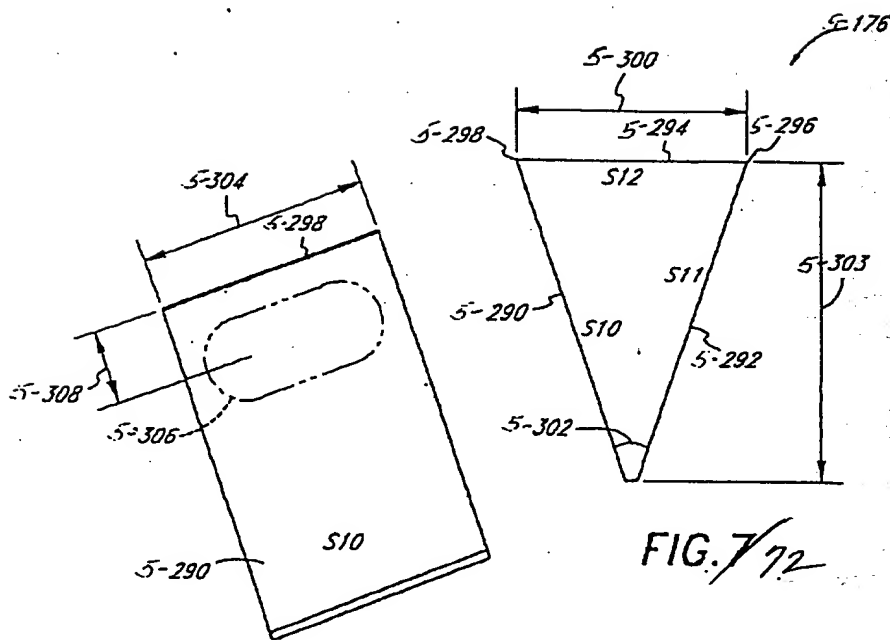


FIG. 70
72a

FIG. 72

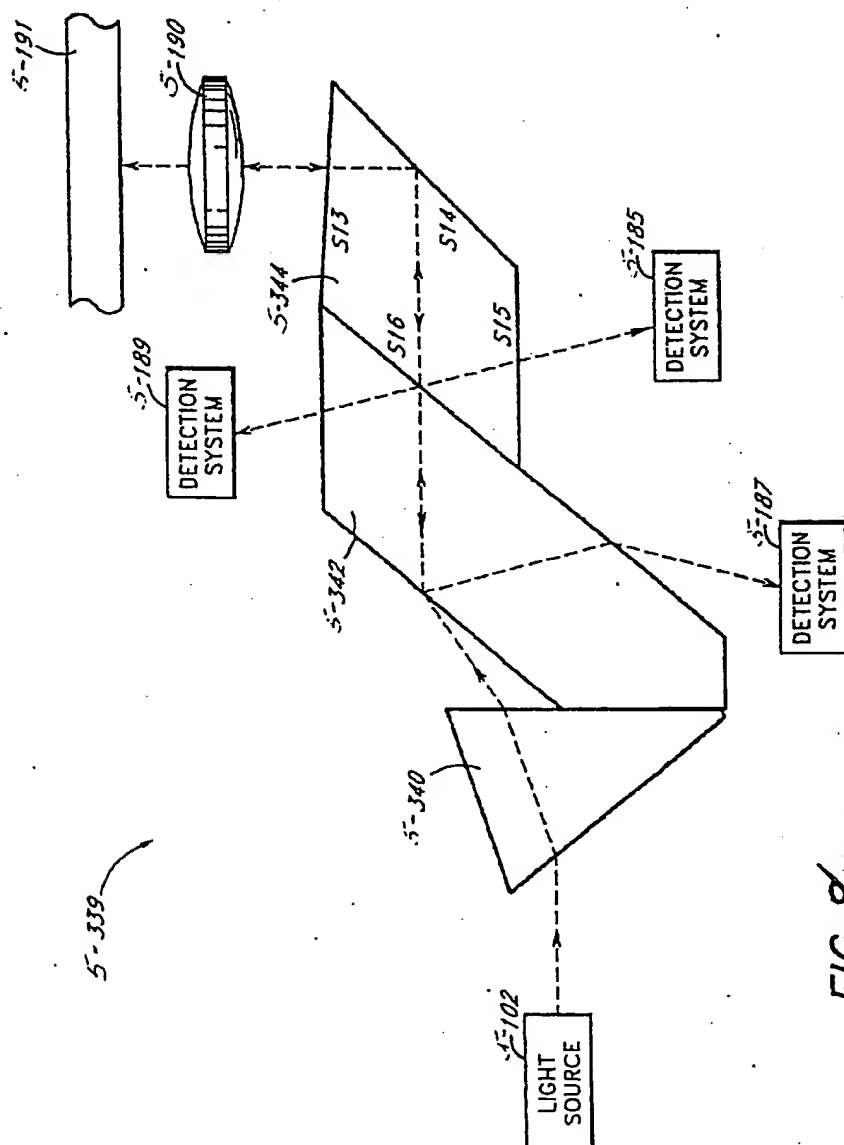
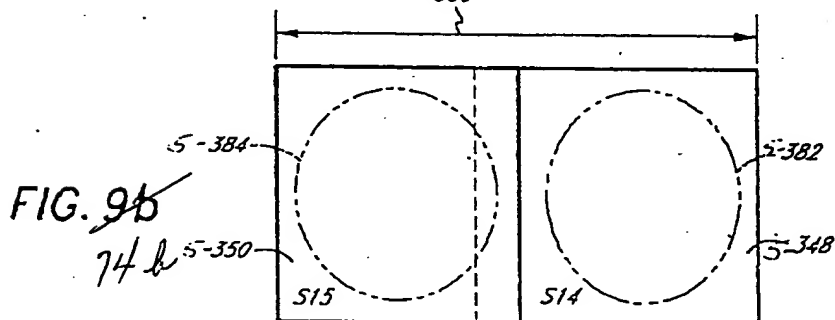
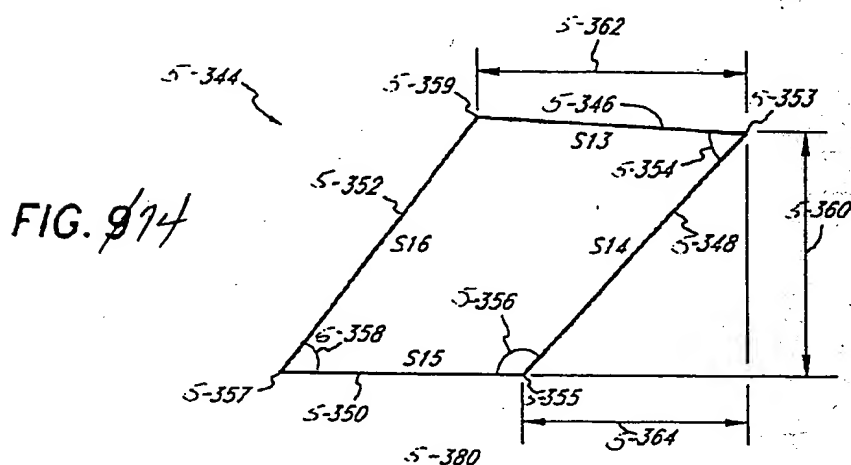
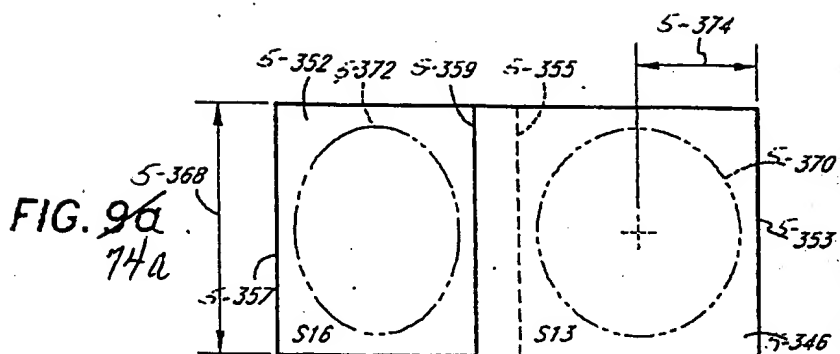
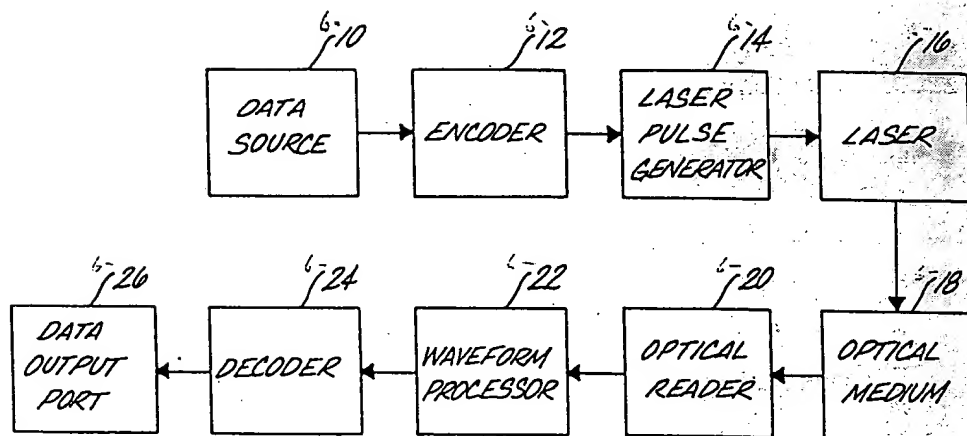


FIG. 8



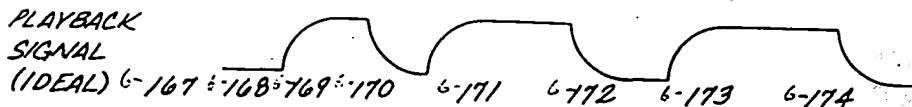
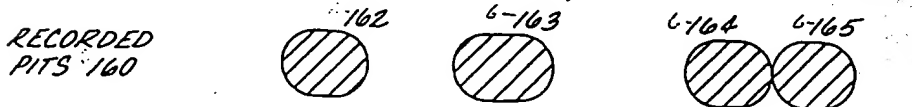
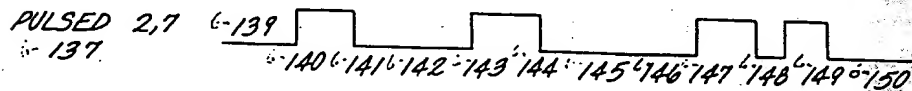
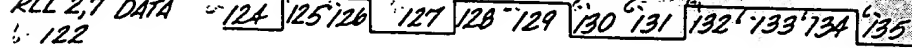
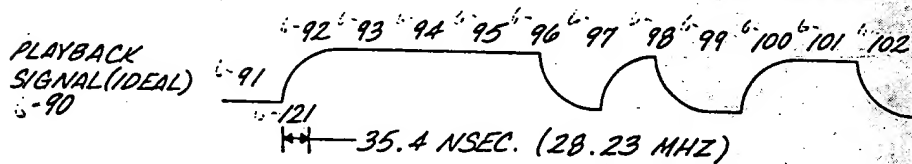
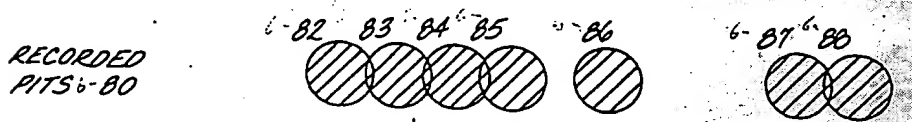
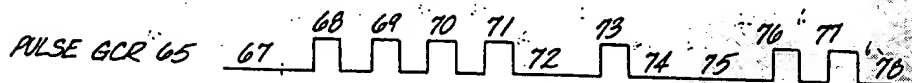
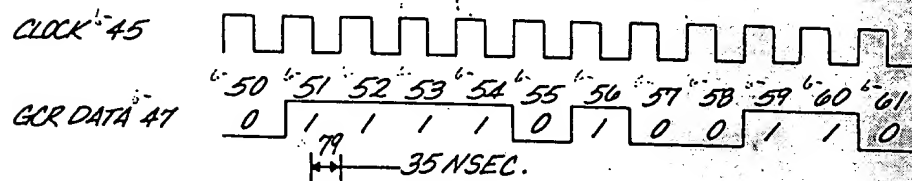
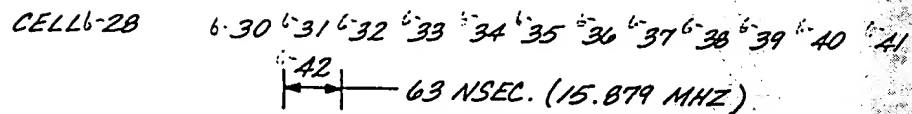
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Fig. ~~1~~ 75



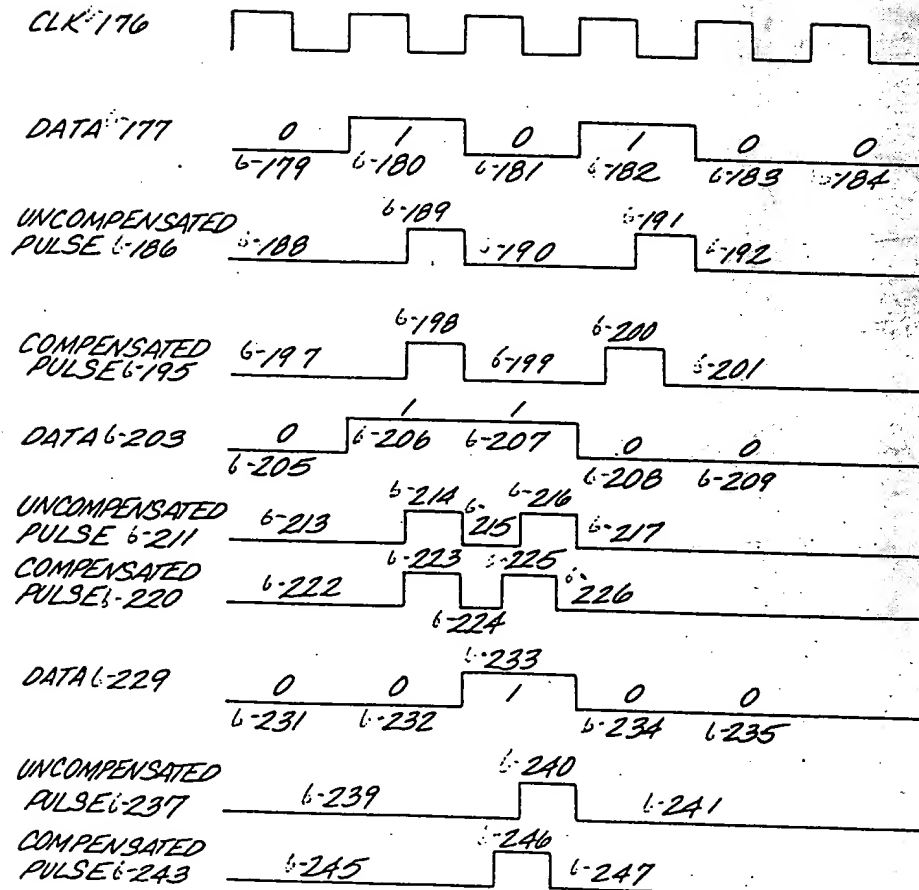
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Fig. 2 ~~75~~ 76



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Fig. 3 #77



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FIG. 77A

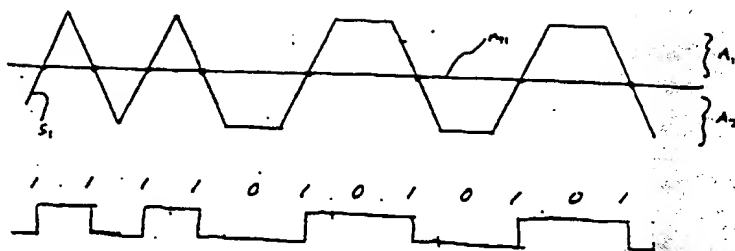
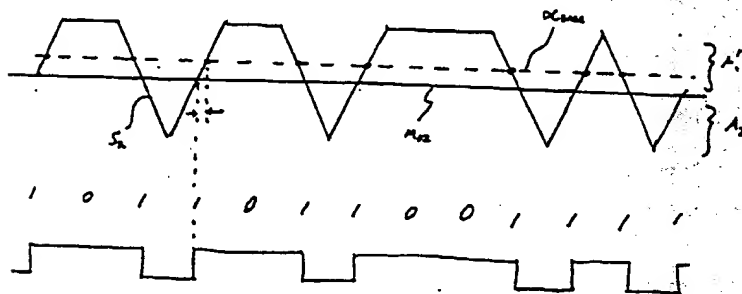
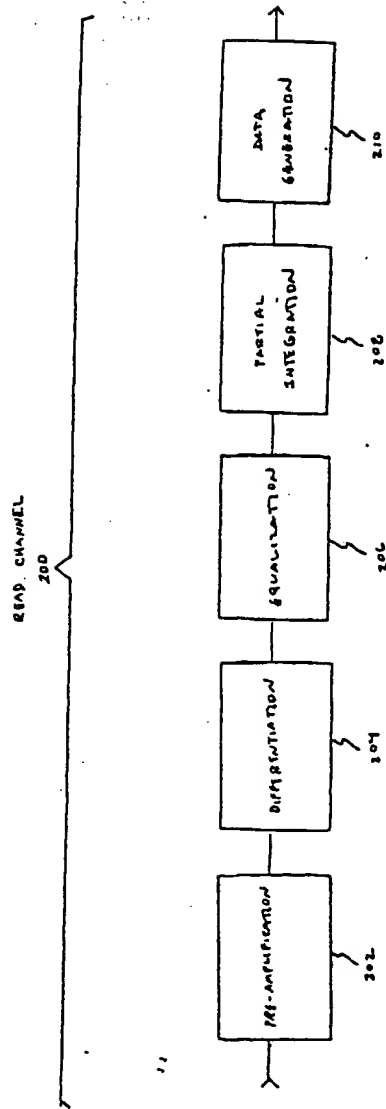


FIG. 77B

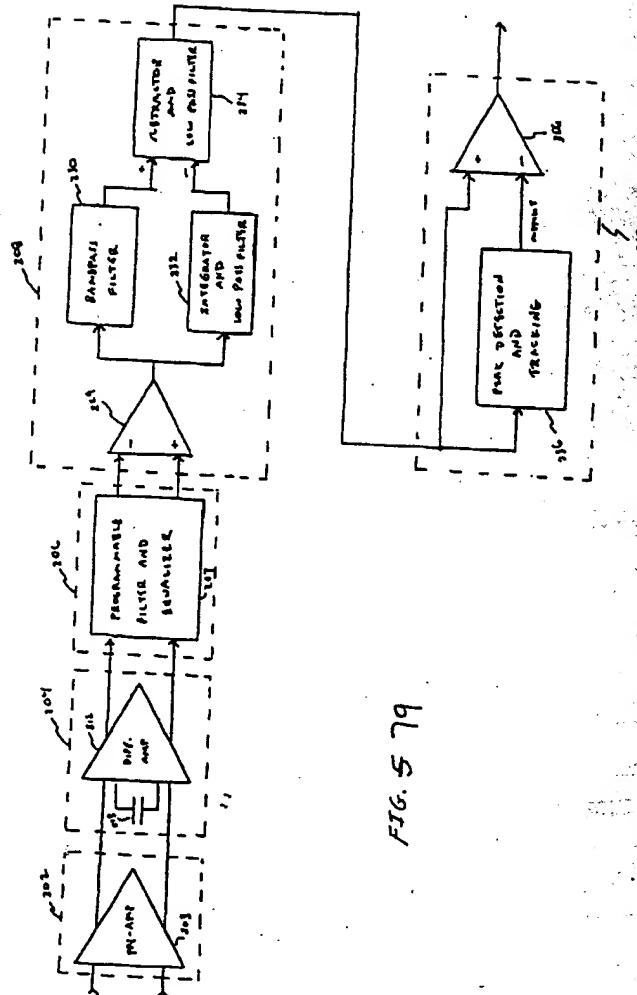


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FIG. 4 78



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 Inventor(s): Noboru Kimura et al.
 Docket No.: 210/079
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REF LEVEL /DIV
 31.500dB 5.000dB
 MARKER 6 797 044.900Hz
 MAG (UDF) 17.456dB

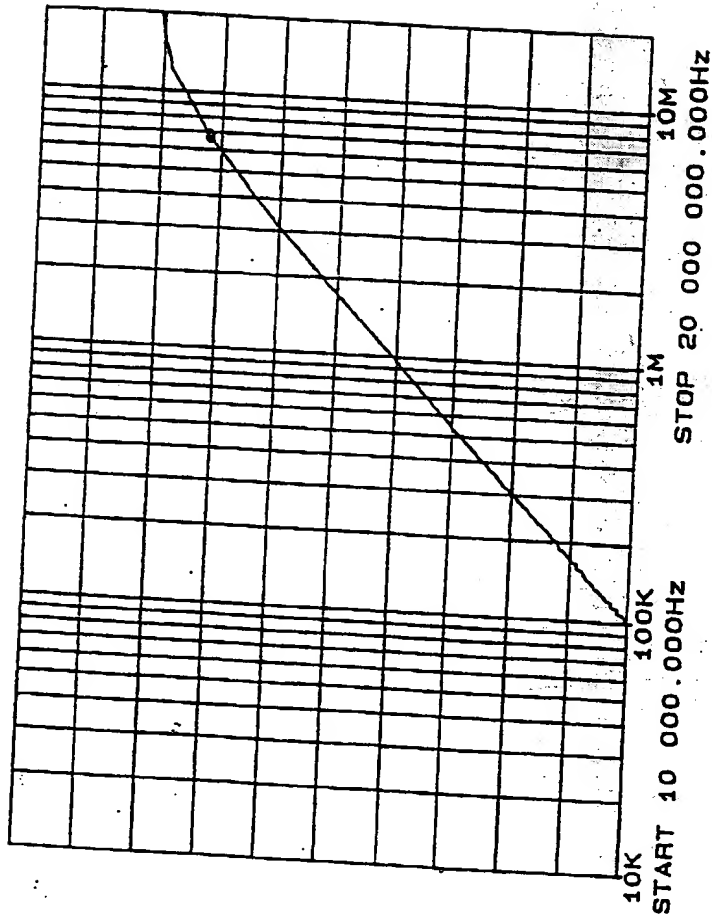


FIG. 80A
 DIFFERENTIATOR

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REF LEVEL /DIV
26.510dB 5.000dB

MARKER 5 620 751.500Hz
MAG (UDF) 7.882dB

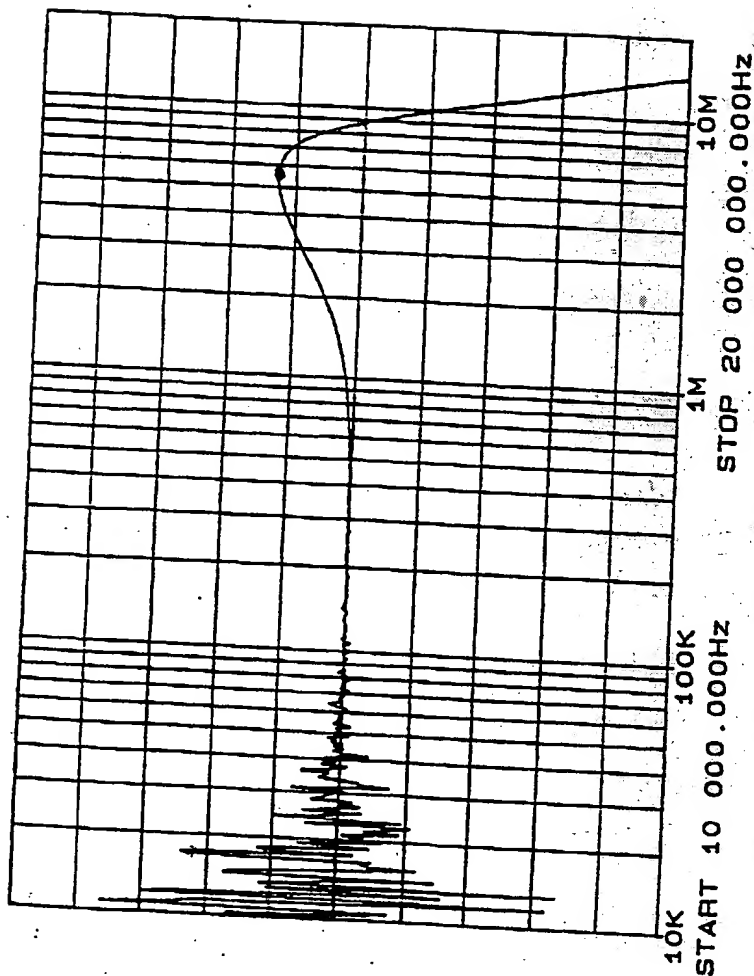


FIG. 4B. 80B
EQUA-1252

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Mail Label No.: B140323711
 Inventor(s): Noboru Kimura et al.
 Docket No.: 210/079
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REF LEVEL /DIV
 9.600dB 6.000dB
 MARKER 5 105 657.600Hz
 MAG (UDF) -26.669dB

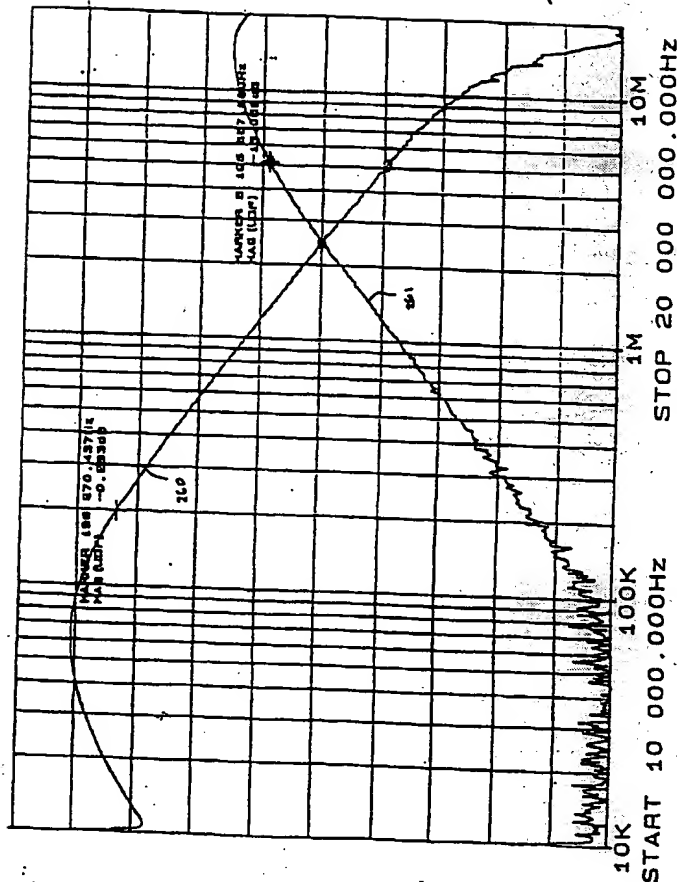


Fig. 60 80 C

3.0 PLOTTING
 8-10-55

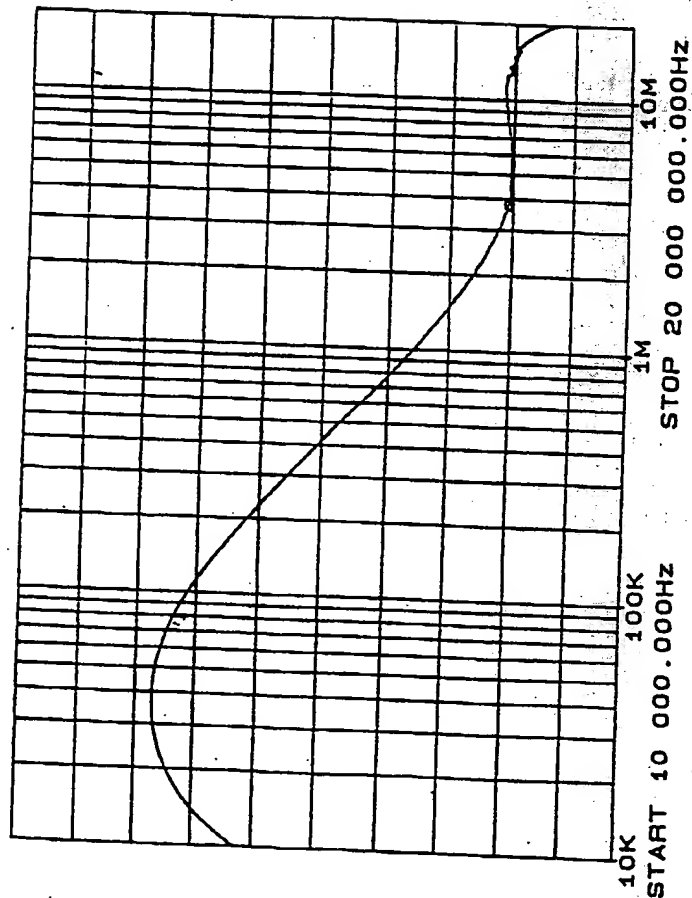
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FIG. 62 80 D
PARTIAL INTEGRATION
STAGE

REF LEVEL /DIV
-2.250dBm 5.000dB
MARKER 3 767 954.400Hz
MAG (UDF) -41.906dBm



START 10 000.000Hz
STOP 20 000 000.000Hz

84

Mail Label No.: B140323711
Inventor(s): Noboru Kinura et al.
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REF LEVEL 31.510dB /DIV 5.000dB
 MARKER 7 064 731.500Hz
 MAG (UDF) 24.277dB

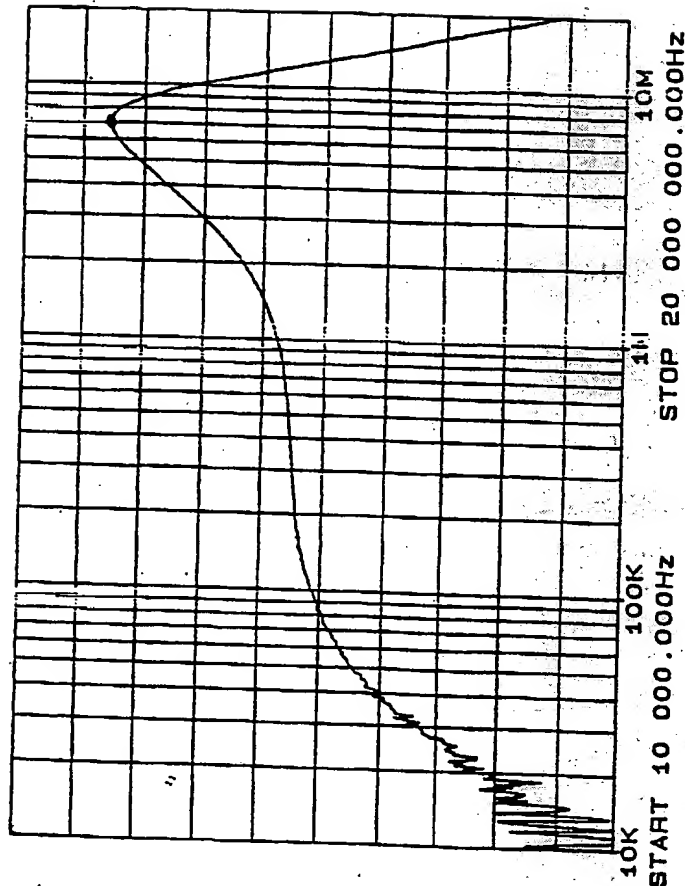
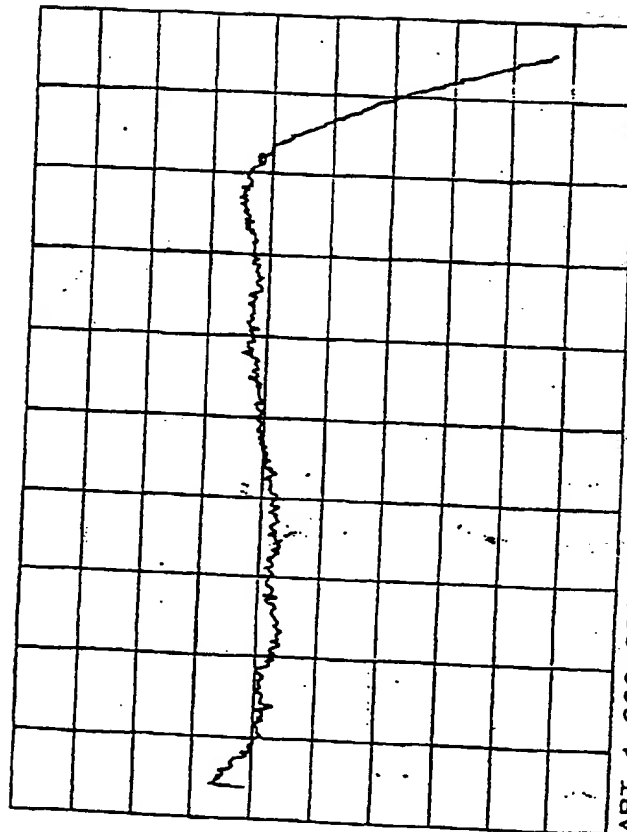


FIG. 6E 80E
 DES REPONSE

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REF LEVEL /DIV MARKER 8 357 500.000HZ
198.00nSEC 5.000nSEC DELAY (UDF) 203.93nSEC



START 1 000 000.000Hz
AMPTD -22.0dBm
STOP 10 000 000.000Hz
DELAY APER 720.0KHz

TOTAL
GROUP DELAY

FIG. 6F 80 F

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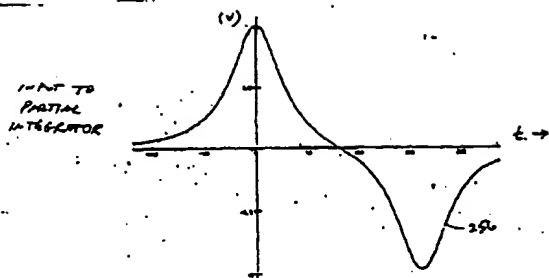
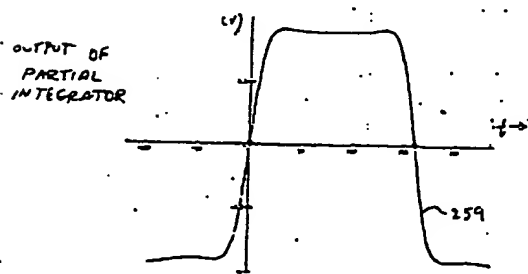
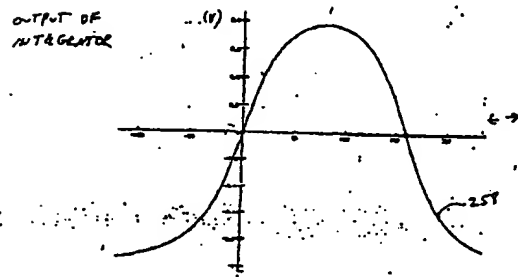
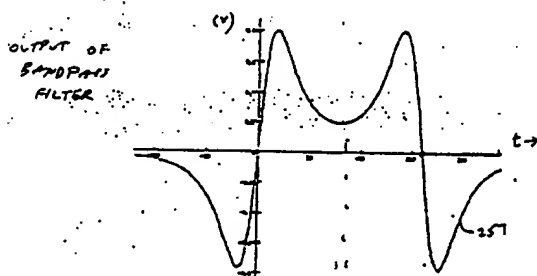


FIG. 6G 80 G



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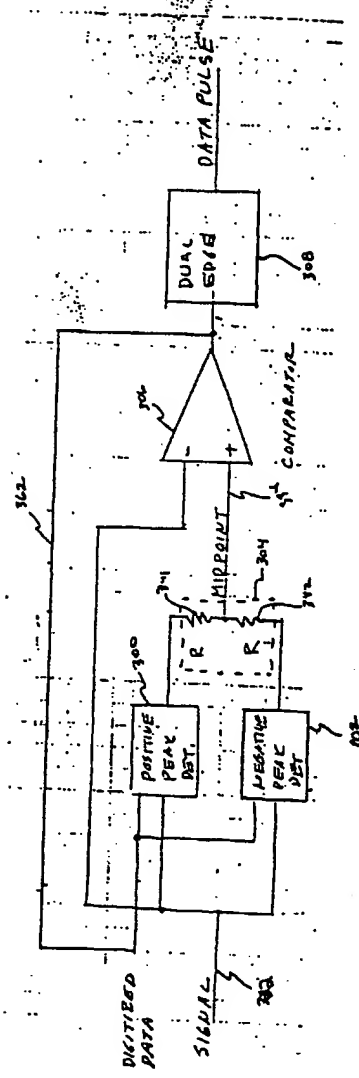
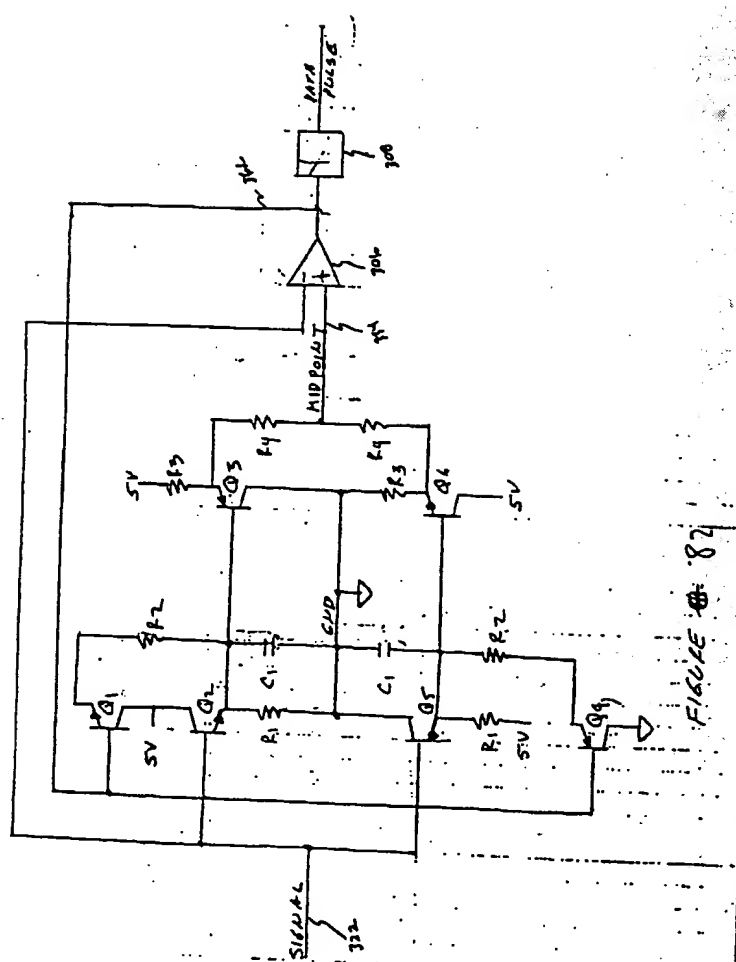


FIG. 7 81

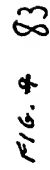
98

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22-141 50 SHIRTS
22-142 100 SHIRTS
22-144 200 SHIRTS

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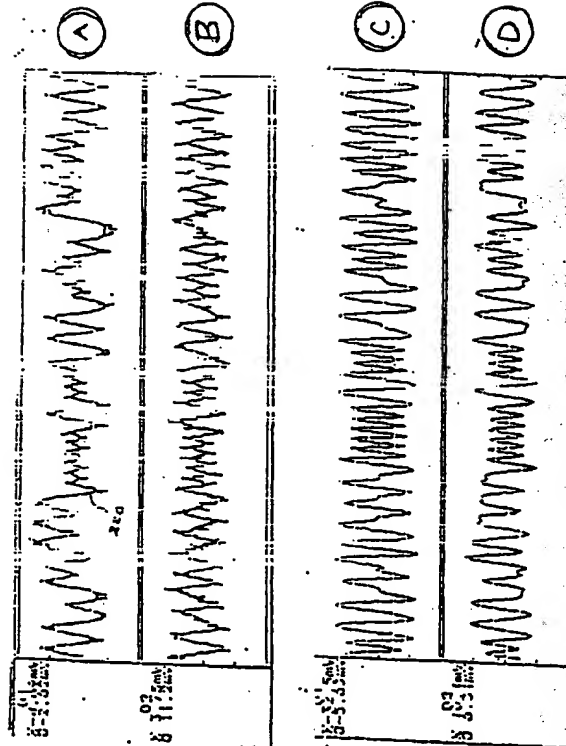


Fig. 40 84

al

SENT BY: Lyon & Lyon L.A.

; 1-19-95 ; 9:07AM ;

Lyon & Lyon L.A. -

08/420899

719 527 3402;# 2/4

Fig. 85

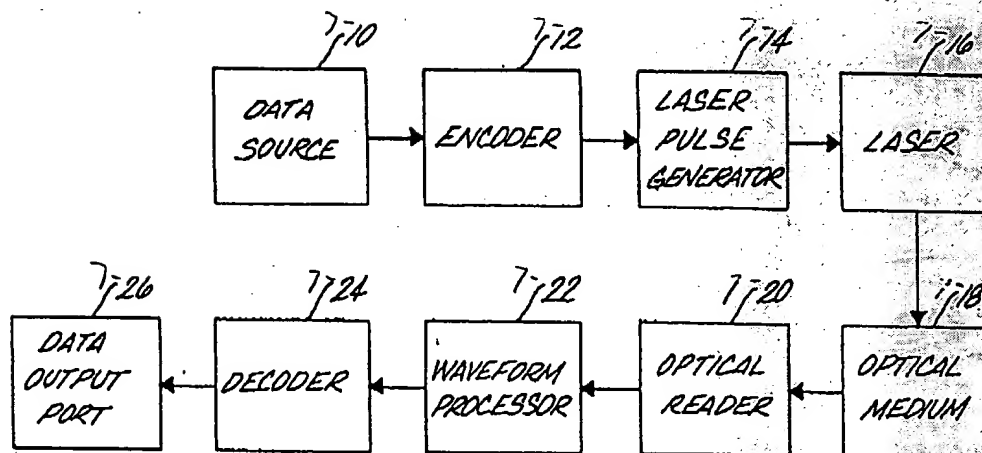
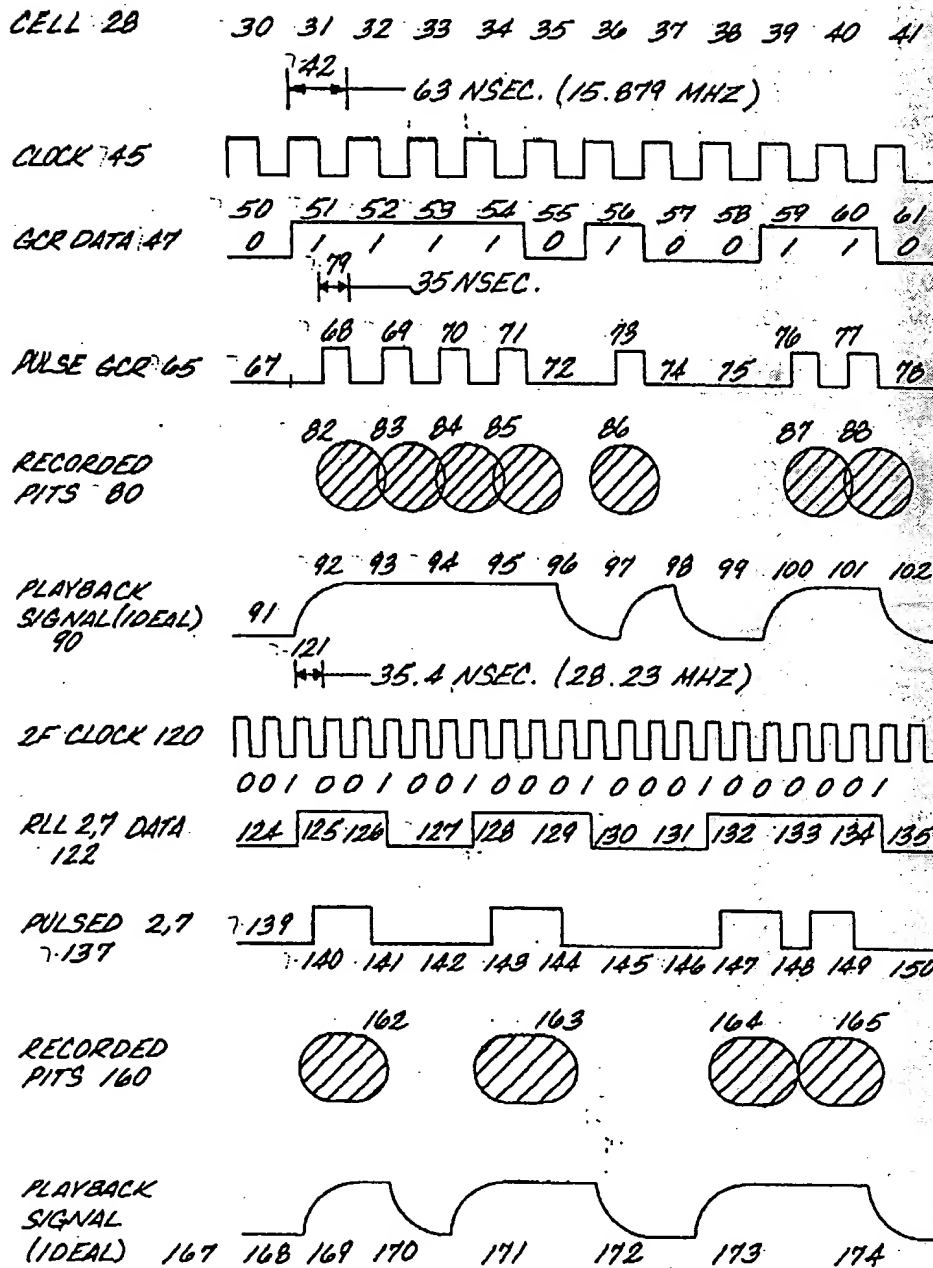


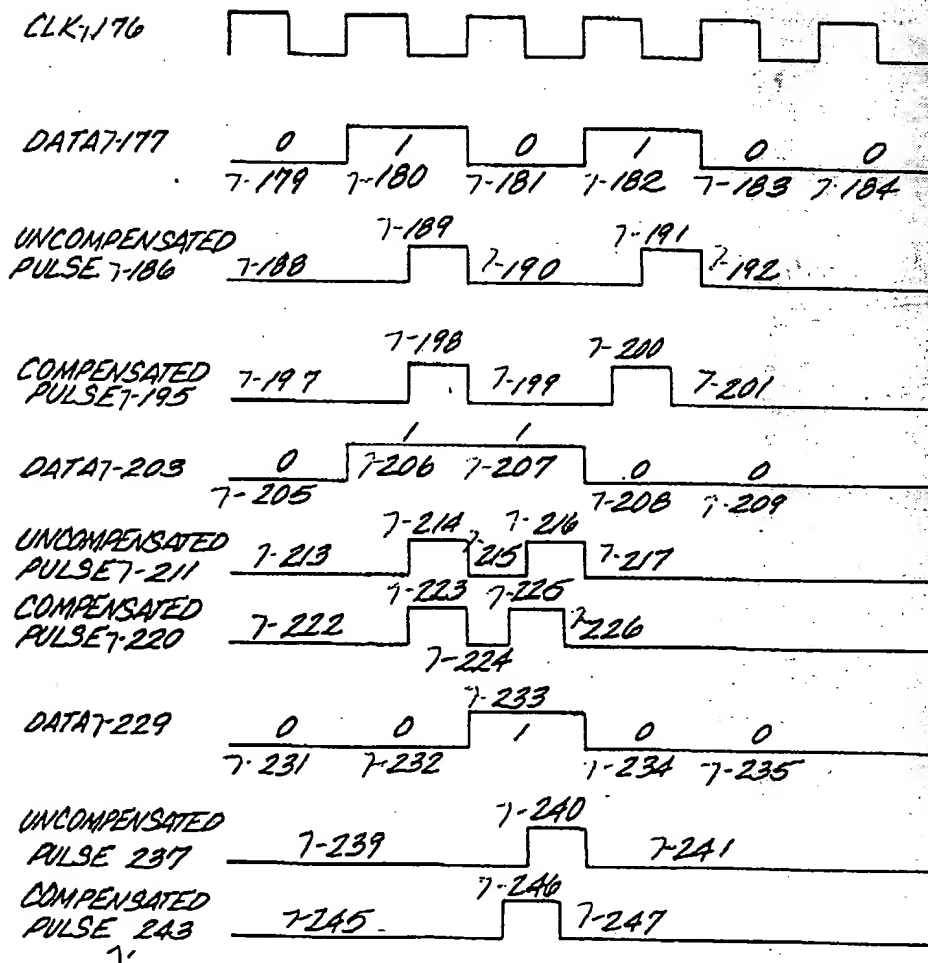
Fig. 2 86

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Fig. 887



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Fig. 5 89

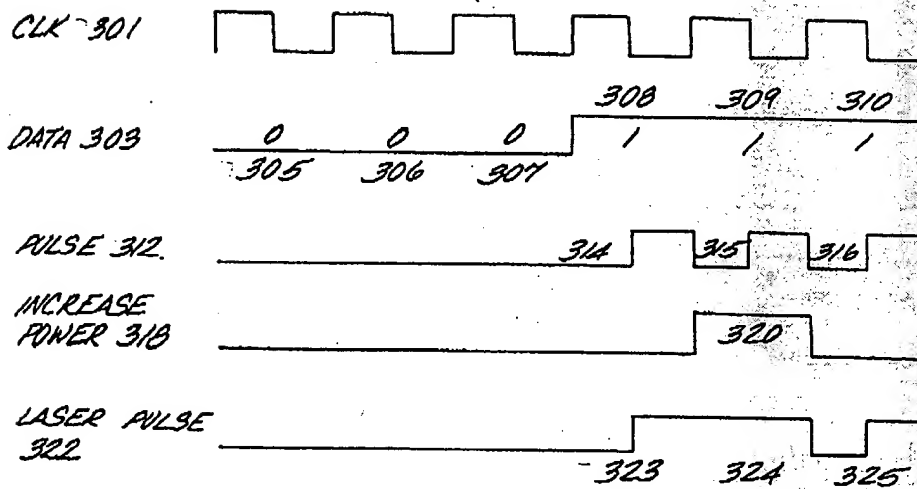


Fig. 7 91

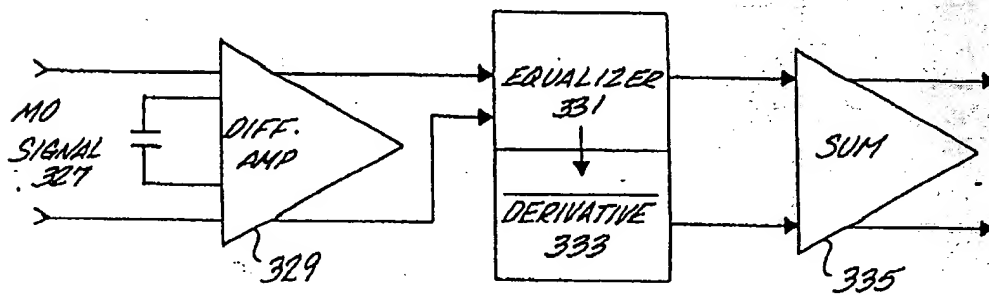


Fig. 90

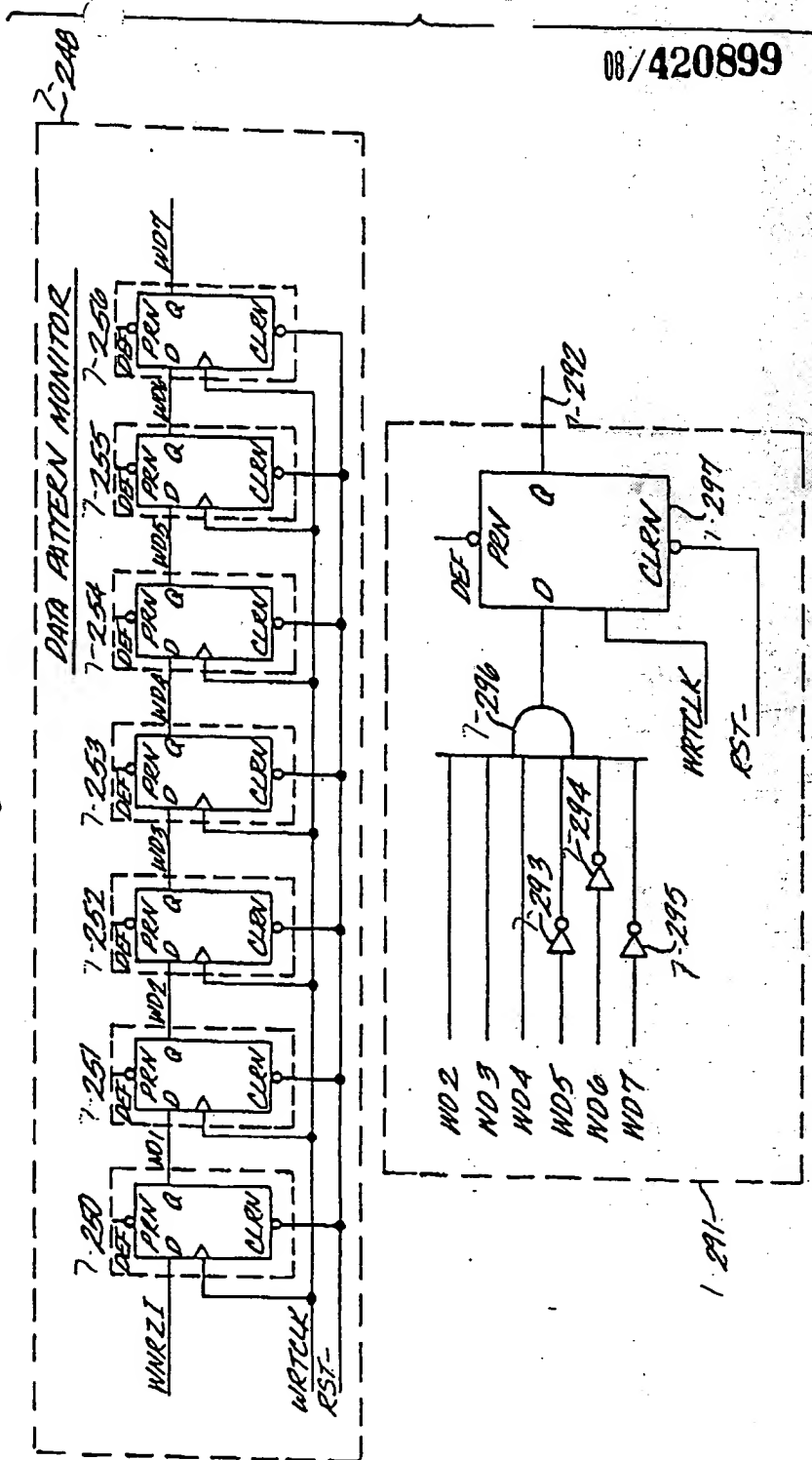


Fig. 8 92

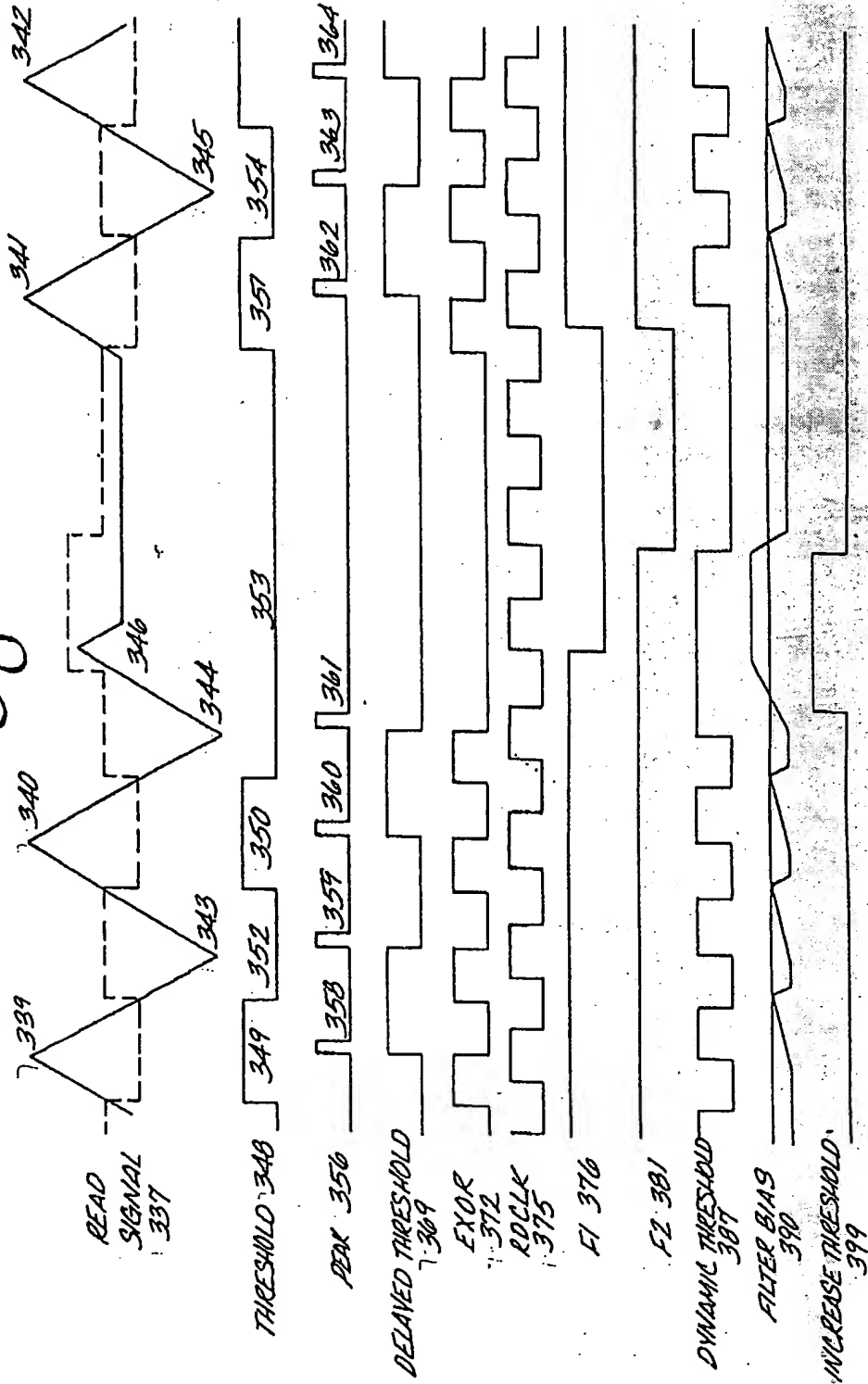
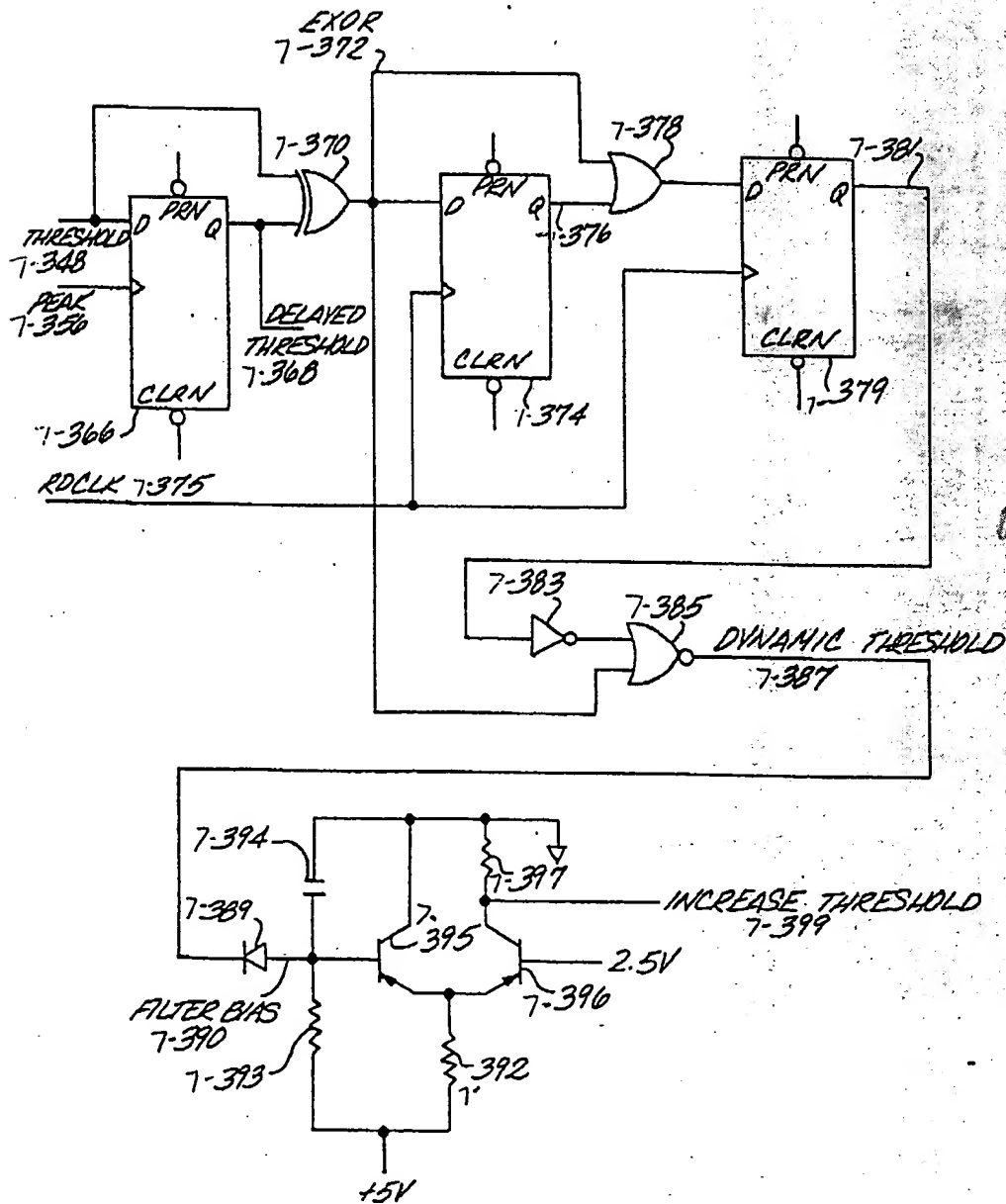
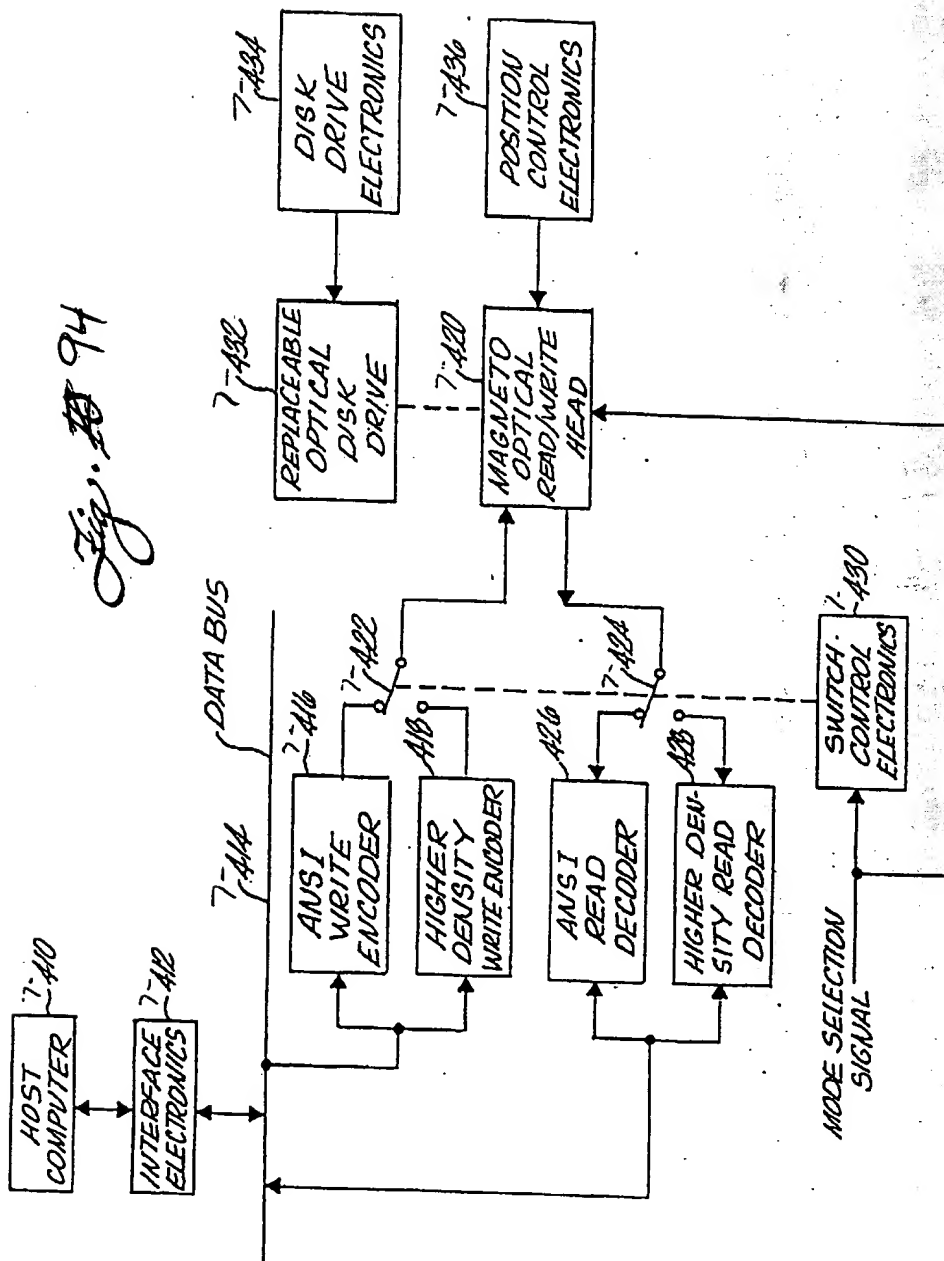


Fig. 93

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SENT BY: Lyon & Lyon L.A.

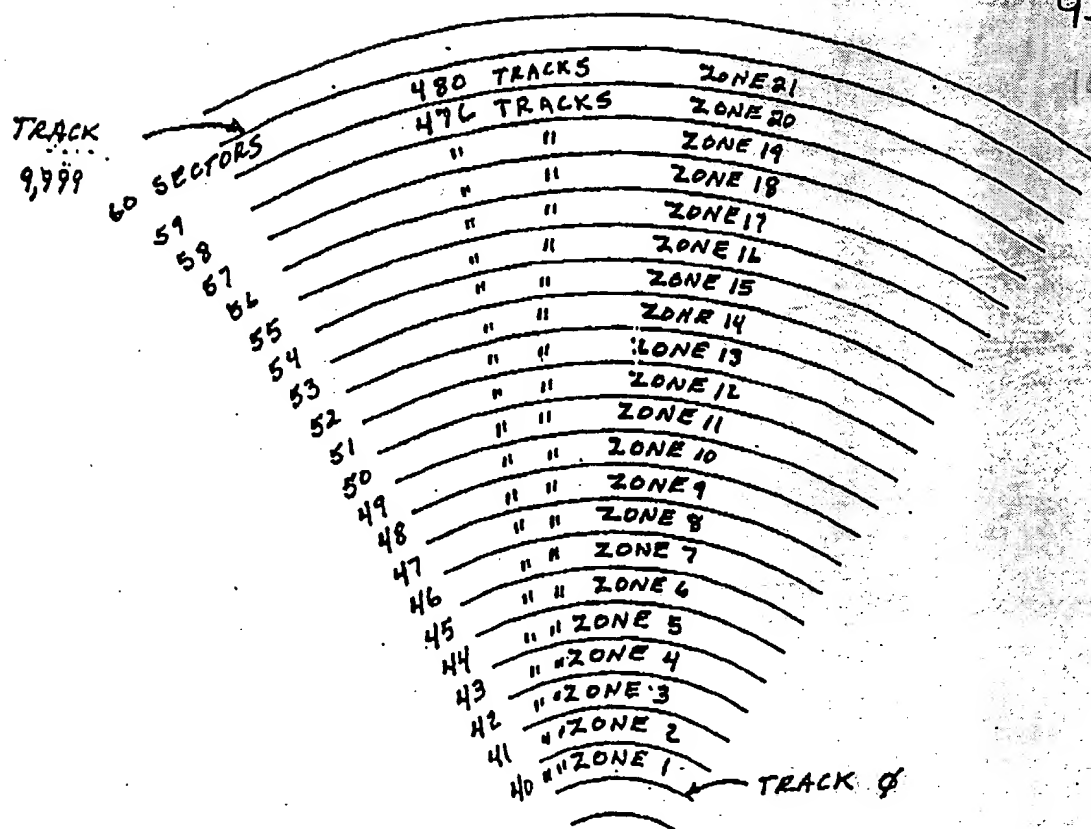
1-19-95 ; 9:07AM ; Lyon & Lyon L.A.

719 527 3402: # 3/ 4

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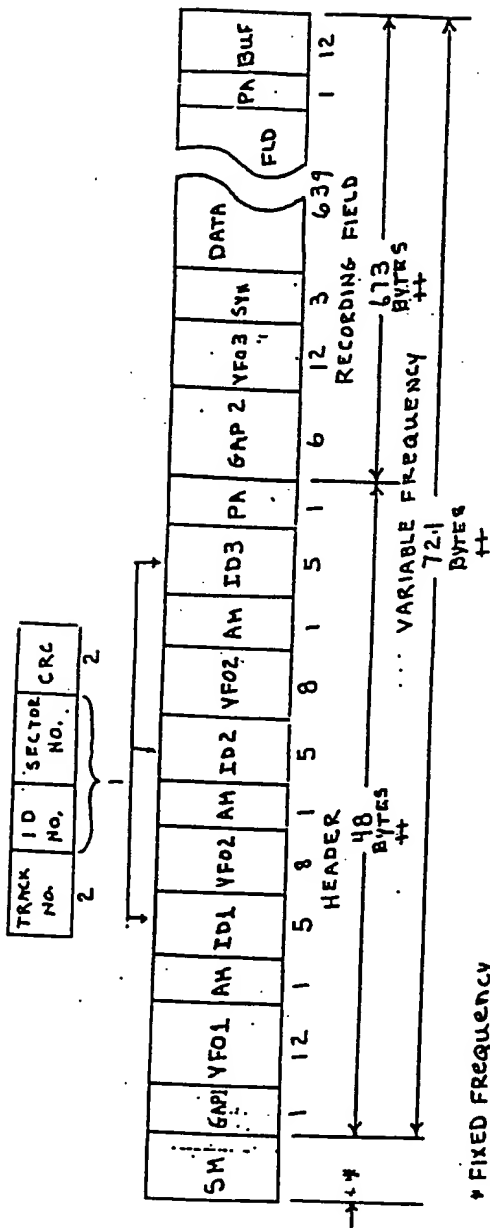
TRACK LAYOUT

FIG. #
95



SECTOR FORMAT

FIG. 96

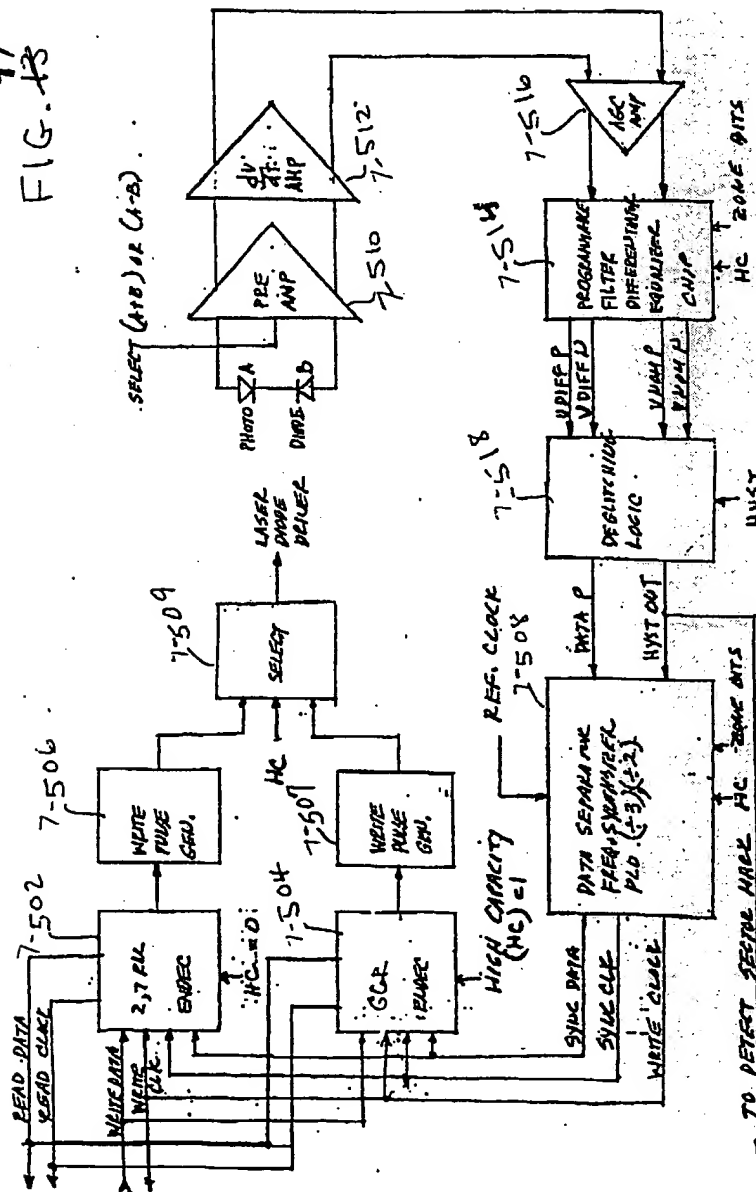


* FIXED FREQUENCY
80 CHANNEL BITS

++ 1 BYTE = 9 CHANNEL BITS

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FIG. 43



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HIGH CAPACITY DRIVE 2400 RPM

ZONE	(ABSOLUTE)	NO. OF SECTORS PER TRACK	NO. OF SEC./ZONE	WRITE FREQ. (Hz)
1	0 — 475	40	19040	10.591
2	476 — 951	41	19516	10.852
3	952 — 1427	42	19992	11.117
4	1428 — 1903	43	20468	11.386
5	1904 — 2379	44	20944	11.656
6	2380 — 2855	45	21420	11.923
7	2856 — 3331	46	21896	12.190
8	3332 — 3807	47	22372	12.467
9	3808 — 4283	48	22848	12.745
10	4284 — 4759	49	23324	12.992
11	4760 — 5235	50	23800	13.257
12	5236 — 5711	51	24276	13.533
13	5712 — 6187	52	24752	13.831
14	6188 — 6663	53	25228	14.076
15	6664 — 7139	54	25704	14.362
16	7140 — 7615	55	26180	14.624
17	7616 — 8091	56	26656	14.914
18	8092 — 8567	57	27132	15.130
19	8568 — 9043	58	27608	15.467
20	9044 — 9519	59	28084	15.694
21	9520 — 9999	60	28560	15.950
			TOTAL SEC. 504960	
			$\times 672 \text{ B/S} =$	
			256.02 MB	

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CRC FOR ID FIELDS

The 16 check bits of the CRC of the ID field shall be computed over the first three bytes of this field. The generator polynomial shall be:

$$G(x) = x^{16} + x^{12} + x^5 + 1.$$

The residual polynomial is defined by:

$$R(x) = \left(\sum_{i=8}^{i=23} \bar{b}_i x^i \right) + \left(\sum_{i=0}^{i=7} b_i x^i \right) x^{16} \bmod G(x).$$

where b_i denotes a bit of the first three bytes and \bar{b}_i an inverted bit. Bit b_{23} is the highest order bit of the first byte.

The contents of the 16 check bits c_k of the CRC are defined by:

$$R_c(x) = \sum_{k=0}^{k=15} c_k x^k.$$

c_{15} is recorded in the highest order bit of the fourth byte in the ID field.

08/420859

8 Bit Byte		Encoded 9 Bit Byte	8 bit Byte		Encoded 9 Bit Byte
Hex	Binary		Hex	Binary	
00	00000000	011001111	40	01000000	010001011
01	00000001	011001001	41	01000001	010001001
02	00000010	001001101	42	01000010	010001010
03	00000011	101100011	43	01000011	010001011
04	00000100	011001010	44	01000100	010001010
05	00000101	101100101	45	01000101	010001011
06	00000110	101100110	46	01000110	010001101
07	00000111	101100111	47	01000111	010001110
08	00001000	011001111	48	01001000	010010111
09	00001001	101101001	49	01001001	010010110
0A	00001010	101101010	4A	01001010	010010101
0B	00001011	101101011	4B	01001011	010010110
0C	00001100	011001110	4C	01001100	010011011
0D	00001101	101101101	4D	01001101	010011010
0E	00001110	101101110	4E	01001110	010011101
0F	00001111	101101111	4F	01001111	010011110
10	00010000	001001011	50	01010000	010101011
11	00010001	001001001	51	01010001	010101010
12	00010010	011001101	52	01010010	010101011
13	00010011	100100011	53	01010011	010101010
14	00010100	001001010	54	01010100	010101011
15	00010101	100100101	55	01010101	010101010
16	00010110	100100110	56	01010110	010101101
17	00010111	100100111	57	01010111	010101110
18	00011000	001001111	58	01011000	010110111
19	00011001	100101001	59	01011001	111100101
1A	00011010	100101010	5A	01011010	010111001
1B	00011011	100101011	5B	01011011	010111010
1C	00011100	001001110	5C	01011100	010111011
1D	00011101	100101101	5D	01011101	110100101
1E	00011110	100101110	5E	01011110	010111101
1F	00011111	100101111	5F	01011111	010111110
20	00100000	101001111	60	01100000	011001111
21	00100001	101001101	61	01100001	011001110
22	00100010	001010010	62	01100010	001100110
23	00100011	001010011	63	01100011	011010010
24	00100100	001010101	64	01100100	011010011
25	00100101	001010110	65	01100101	011010010
26	00100110	001010111	66	01100110	011010101
27	00100111	001010111	67	01100111	011010110
28	00101000	101001011	68	01101000	011010111
29	00101001	001011001	69	01101001	111100110
2A	00101010	001011010	6A	01101010	011011001
2B	00101011	001011011	6B	01101011	011011010
2C	00101100	101001010	6C	01101100	011011011
2D	00101101	001011101	6D	01101101	110100110
2E	00101110	001011110	6E	01101110	011011101
2F	00101111	001011111	6F	01101111	011011110
30	00110000	011100011	70	01110000	011011111
31	00110001	001100011	71	01110001	011100111
32	00110010	001100010	72	01110010	001100110
33	00110011	001100011	73	01110011	011100111
34	00110100	001100011	74	01110100	011100110
35	00110101	001101010	75	01110101	010100111
36	00110110	001101011	76	01110110	011101011
37	00110111	001101011	77	01110111	011101010
38	00111000	111100011	78	01111000	011101011
39	00111001	001111001	79	01111001	111100111
3A	00111010	001111010	7A	01111010	011111001
3B	00111011	001111011	7B	01111011	011111010
3C	00111100	110100011	7C	01111100	011111011
3D	00111101	001111101	7D	01111101	110100111
3E	00111110	001111110	7E	01111110	011111101
3F	00111111	001111111	7F	01111111	011111110
Position in byte	8 1	9 1	Position in byte	8 1	9 1

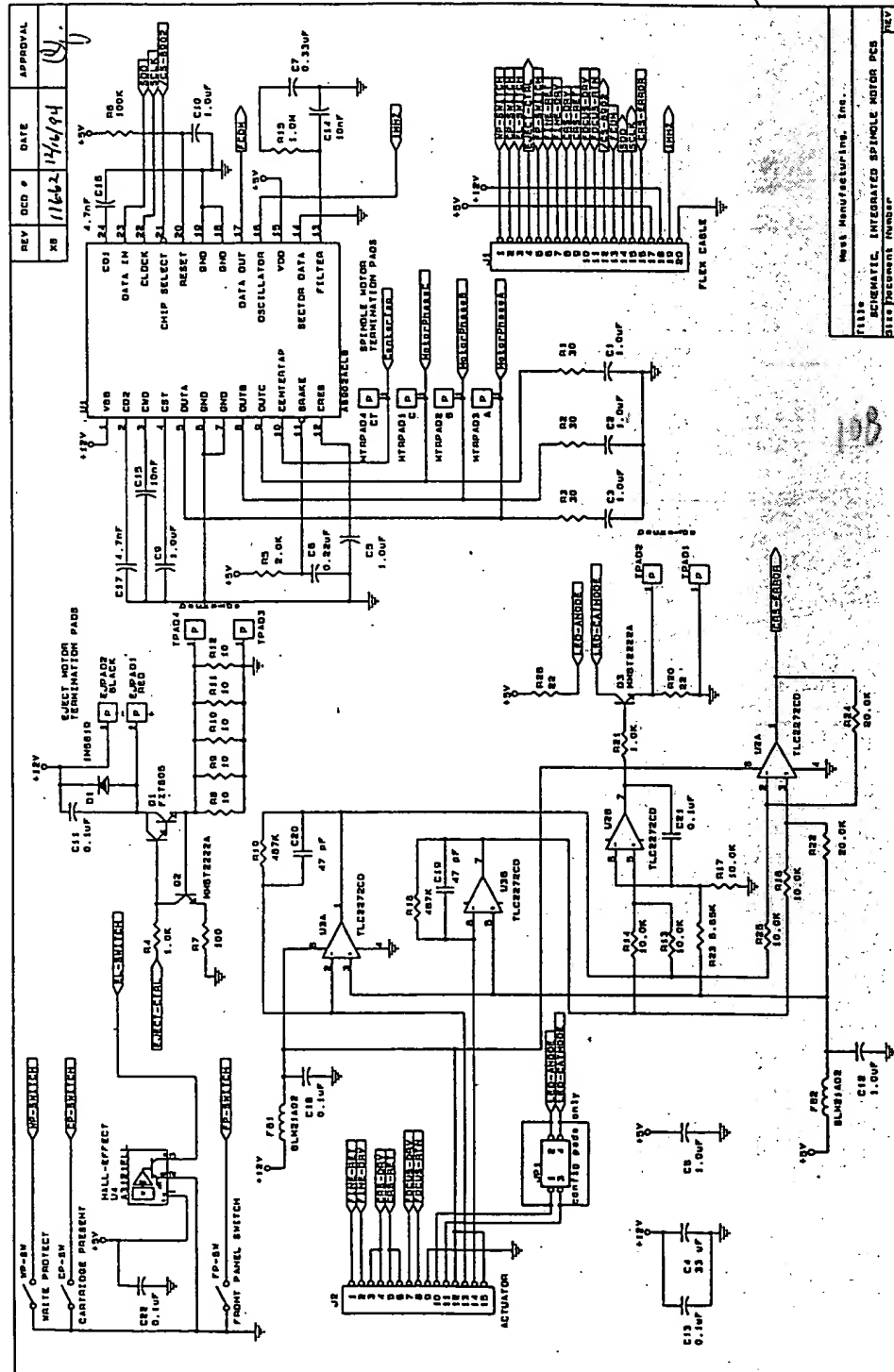
8-bit Byte			Encoded		
Hex	Binary		9-bit Byte		
80	10000000		111001011		
81	10000001		111001001		
82	10000010		100010010		
83	10000011		100010011		
84	10000100		111001010		
85	10000101		100010101		
86	10000110		100010110		
87	10000111		100010111		
88	10001000		111001111		
89	10001001		100011001		
8A	10001010		100011010		
8B	10001011		100011011		
8C	10001100		111001110		
8D	10001101		100011101		
8E	10001110		100011110		
8F	10001111		100011111		
90	10010000		011101001		
91	10010001		001101001		
92	10010010		100110010		
93	10010011		100110011		
94	10010100		010101001		
95	10010101		100110101		
96	10010110		100110110		
97	10010111		100110111		
98	10011000		111101001		
99	10011001		100111001		
9A	10011010		100111010		
9B	10011011		100111011		
9C	10011100		110101001		
9D	10011101		100111101		
9E	10011110		100111110		
9F	10011111		100111111		
A0	10100000		011101010		
A1	10100001		001101010		
A2	10100010		101010010		
A3	10100011		101010011		
A4	10100100		010101010		
A5	10100101		101010101		
A6	10100110		101010110		
A7	10100111		101010111		
A8	10101000		111101010		
A9	10101001		101011001		
AA	10101010		101011010		
AB	10101011		101011011		
AC	10101100		110101010		
AD	10101101		101011101		
AE	10101110		101011110		
AF	10101111		101011111		
B0	10110000		011101011		
B1	10110001		001101011		
B2	10110010		101110010		
B3	10110011		101110011		
B4	10110100		010101011		
B5	10110101		101110101		
B6	10110110		101110110		
B7	10110111		101110111		
B8	10111000		111101011		
B9	10111001		101111001		
BA	10111010		101111010		
BB	10111011		101111011		
BC	10111100		110101011		
BD	10111101		101111101		
BE	10111110		101111110		
BF	10111111		101111111		
Position in byte	8	1	9	1	

8-bit Byte			Encoded		
Hex	Binary		9-bit Byte		
C0	11000000		110001011		
C1	11000001		110001001		
C2	11000010		110001010		
C3	11000011		110001011		
C4	11000100		110001010		
C5	11000101		110001011		
C6	11000110		110001010		
C7	11000111		110001011		
CA	11001000		110001111		
CB	11001001		110001101		
CC	11001010		110011010		
CD	11001011		110011011		
CE	11001100		110011101		
CF	11001101		110011110		
D0	11001110		110011111		
D1	11010000		011101101		
D2	11010001		001101101		
D3	11010010		110110010		
D4	11010011		110110011		
D5	11010100		010101101		
D6	11010101		110110101		
D7	11010110		110110110		
D8	11010111		110110111		
D9	11011000		111101101		
DA	11011001		110111001		
DB	11011010		110111010		
DC	11011011		110111011		
DD	11011100		110111101		
DE	11011101		110111110		
DF	11011110		110111111		
E0	11011111		110111111		
E1	11100000		011101110		
E2	11100001		001101110		
E3	11100010		111010010		
E4	11100011		111010011		
E5	11100100		010101110		
E6	11100101		111010101		
E7	11100110		111010110		
E8	11100111		111010111		
E9	11101000		111101110		
EA	11101001		111011001		
EB	11101010		111011010		
EC	11101011		111011011		
ED	11101100		111011101		
EE	11101101		111011110		
EF	11101110		111011111		
F0	11101111		111011111		
F1	11110000		011101111		
F2	11110001		001101111		
F3	11110010		111110010		
F4	11110011		111110011		
F5	11110100		010101111		
F6	11110101		111110101		
F7	11110110		111110110		
F8	11110111		111110111		
F9	11111000		111110111		
FA	11111001		111111001		
FB	11111010		111111010		
FC	11111011		111111011		
FD	11111100		110101111		
FE	11111101		111111101		
FF	11111110		111111110		
	11111111		111111111		
Position in byte	8	1	9	1	

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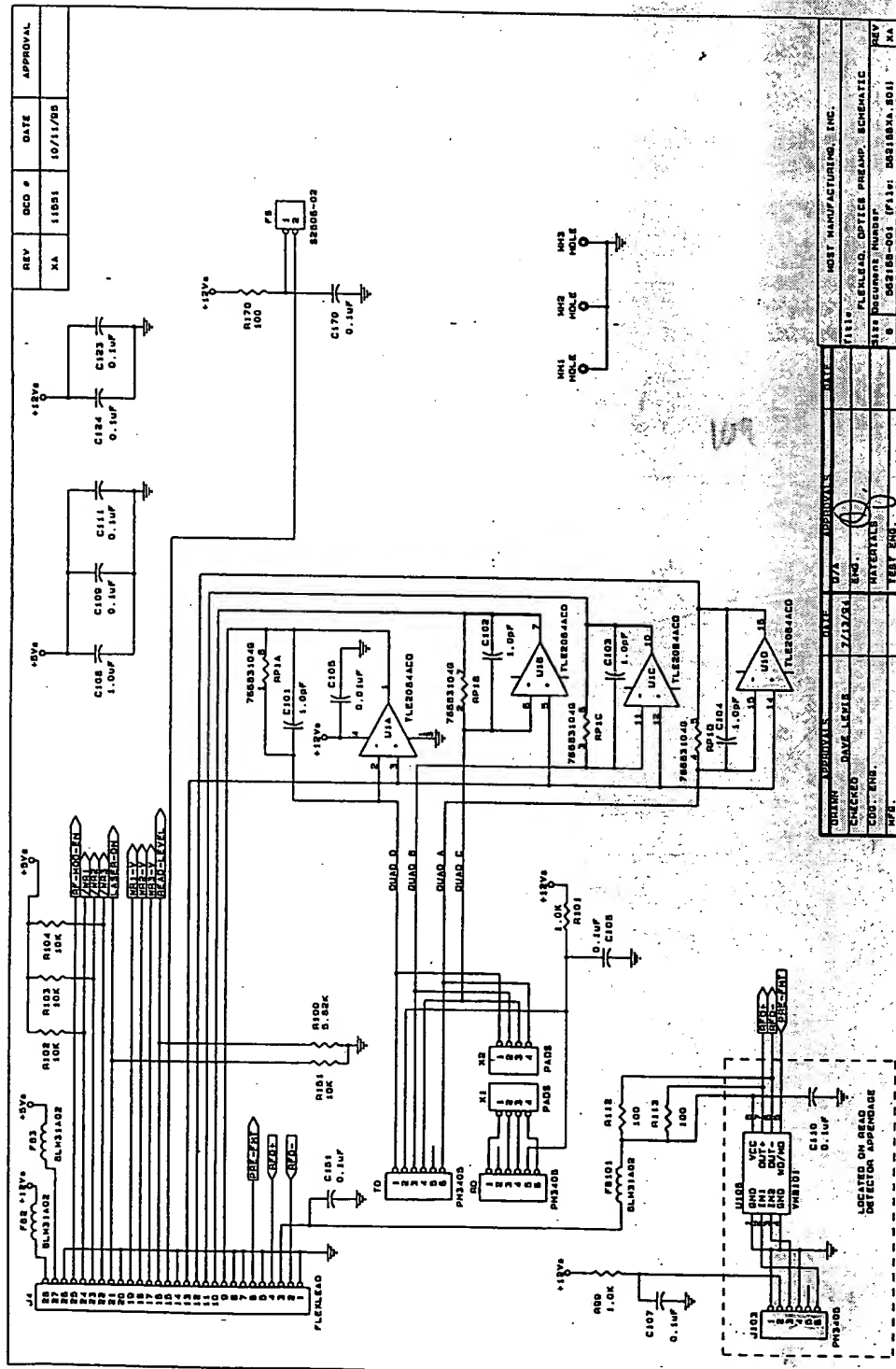
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FIG. 101



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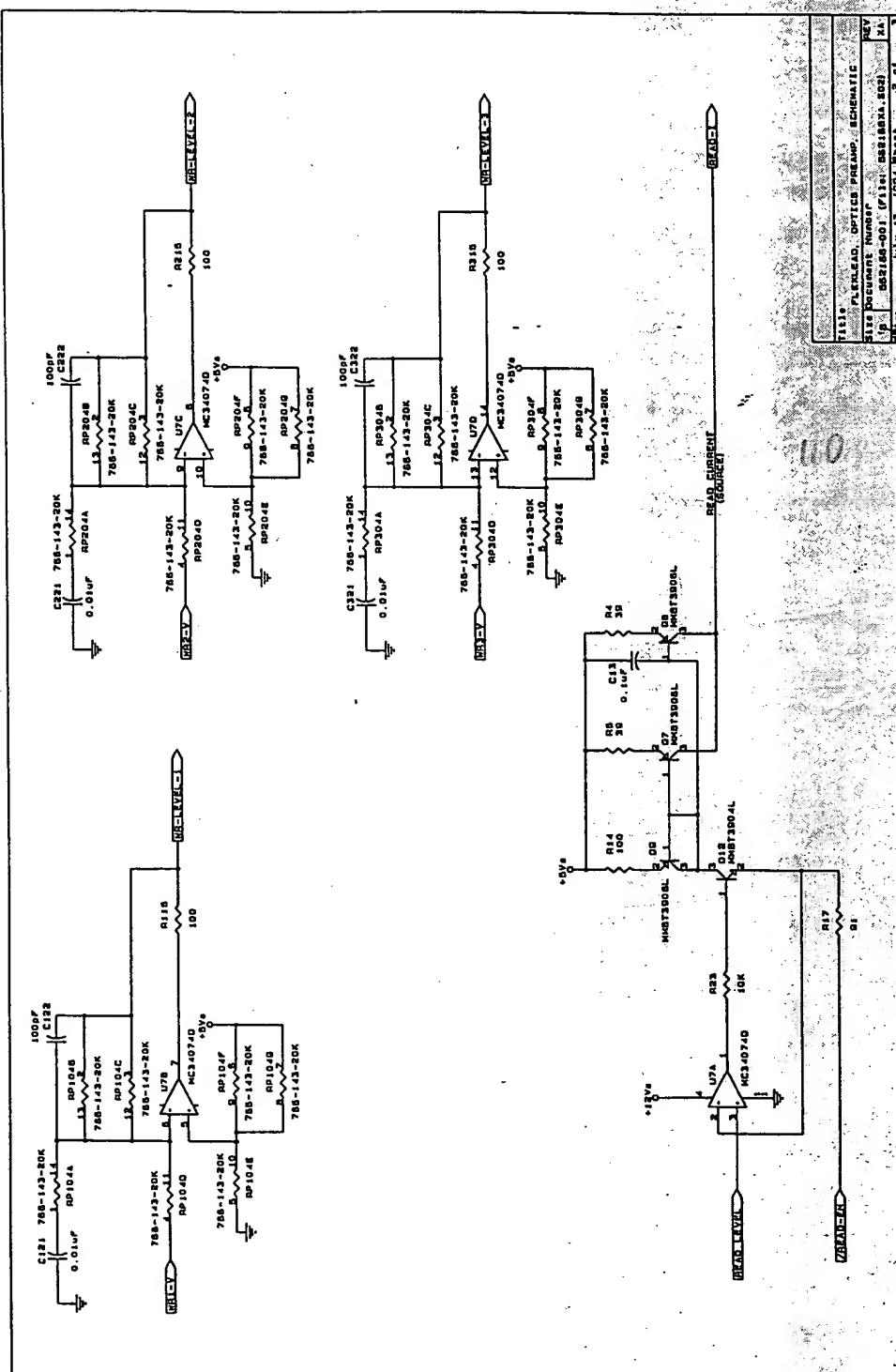
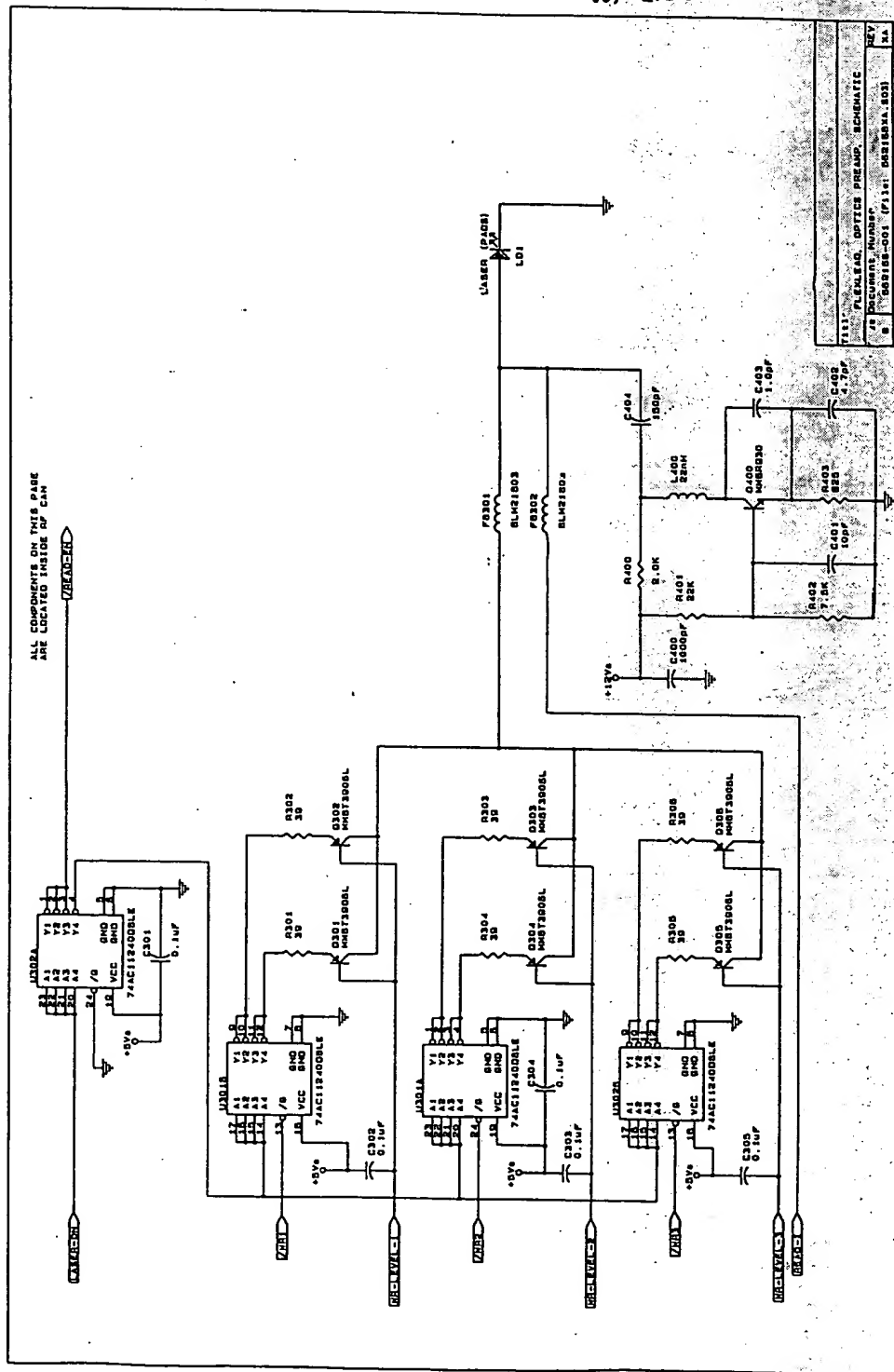


FIG. 104



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FIG. 104	LASER PREAMP, SCHEMATIC
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APP'D.	10/11/81

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ALL COMPONENTS ON THIS PAGE
ARE LOCATED INSIDE RF CAN

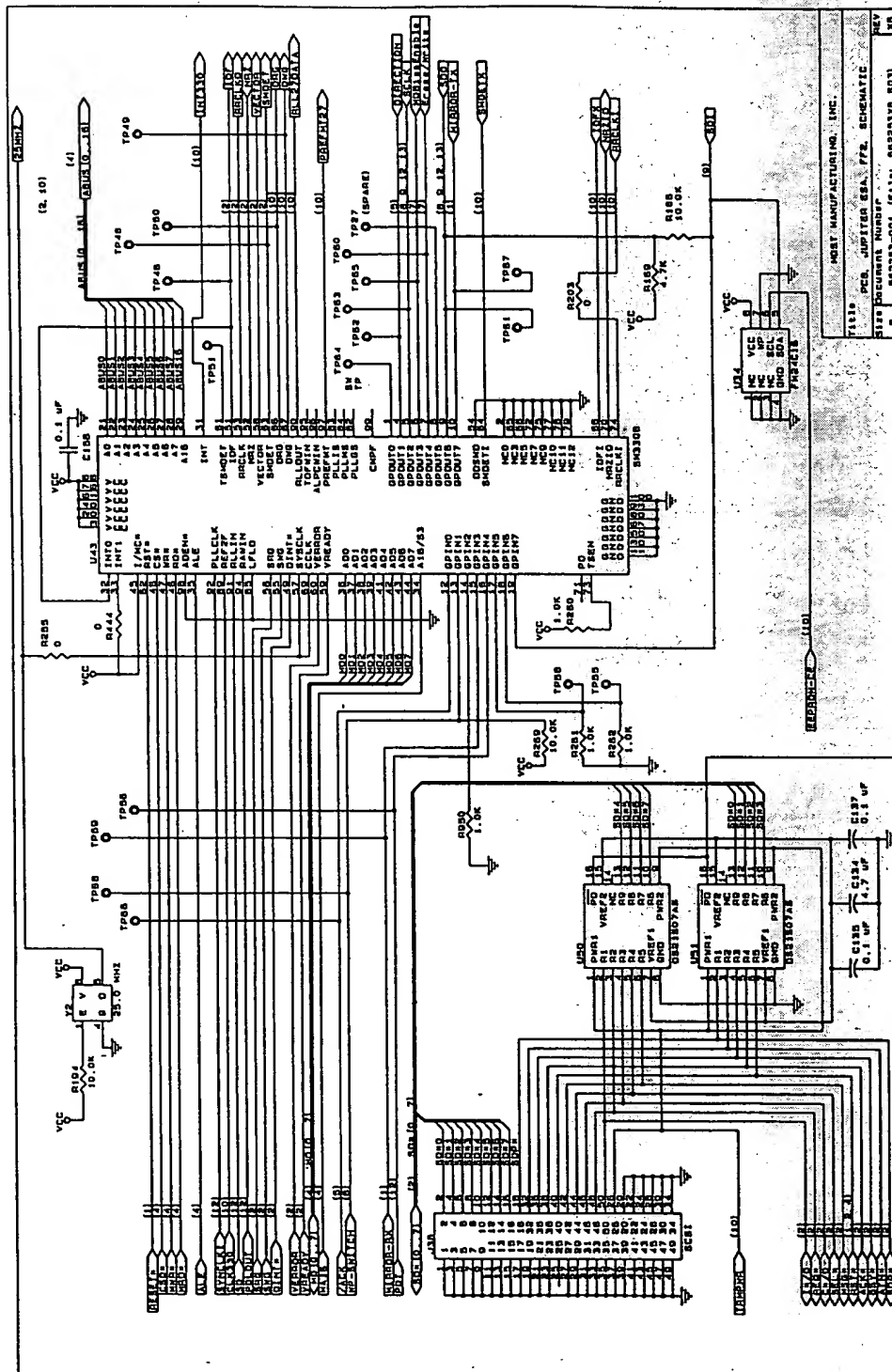
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FILE	Document Number
FILE	582168-001 (File: 582168XA.503)
FILE	October 11 1984 Sheet 3 of 3

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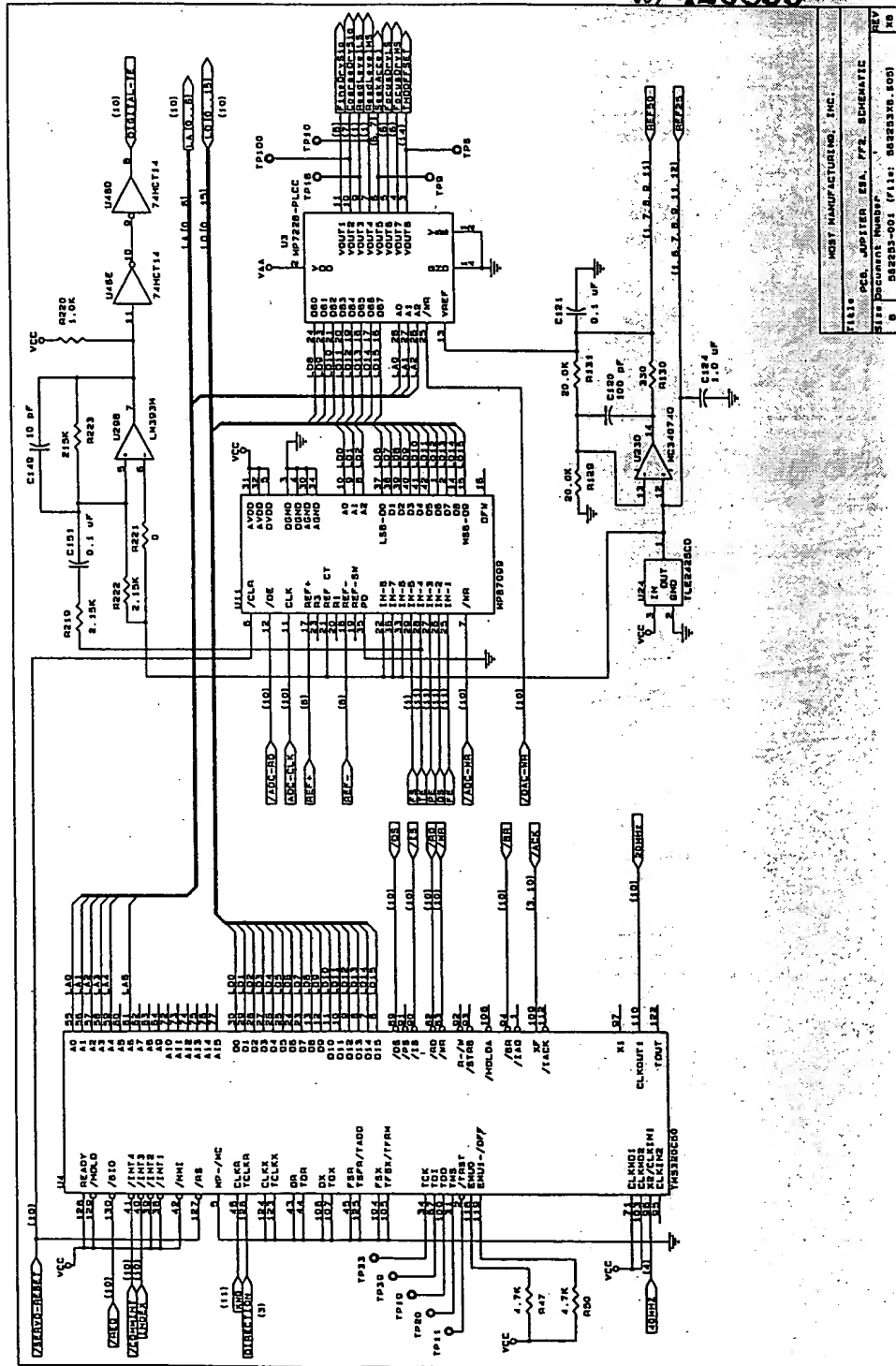
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8	582253-001	(Title: 082253MB.004)	XP

FIG. 110



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MOBY MANUFACTURING, INC.
 FILE: PCS_ADAPTER_EIA_FF2_SCHEMATIC
 Size: Document Number
 8 882233-001 (F11: 882233X8.109) REV 10

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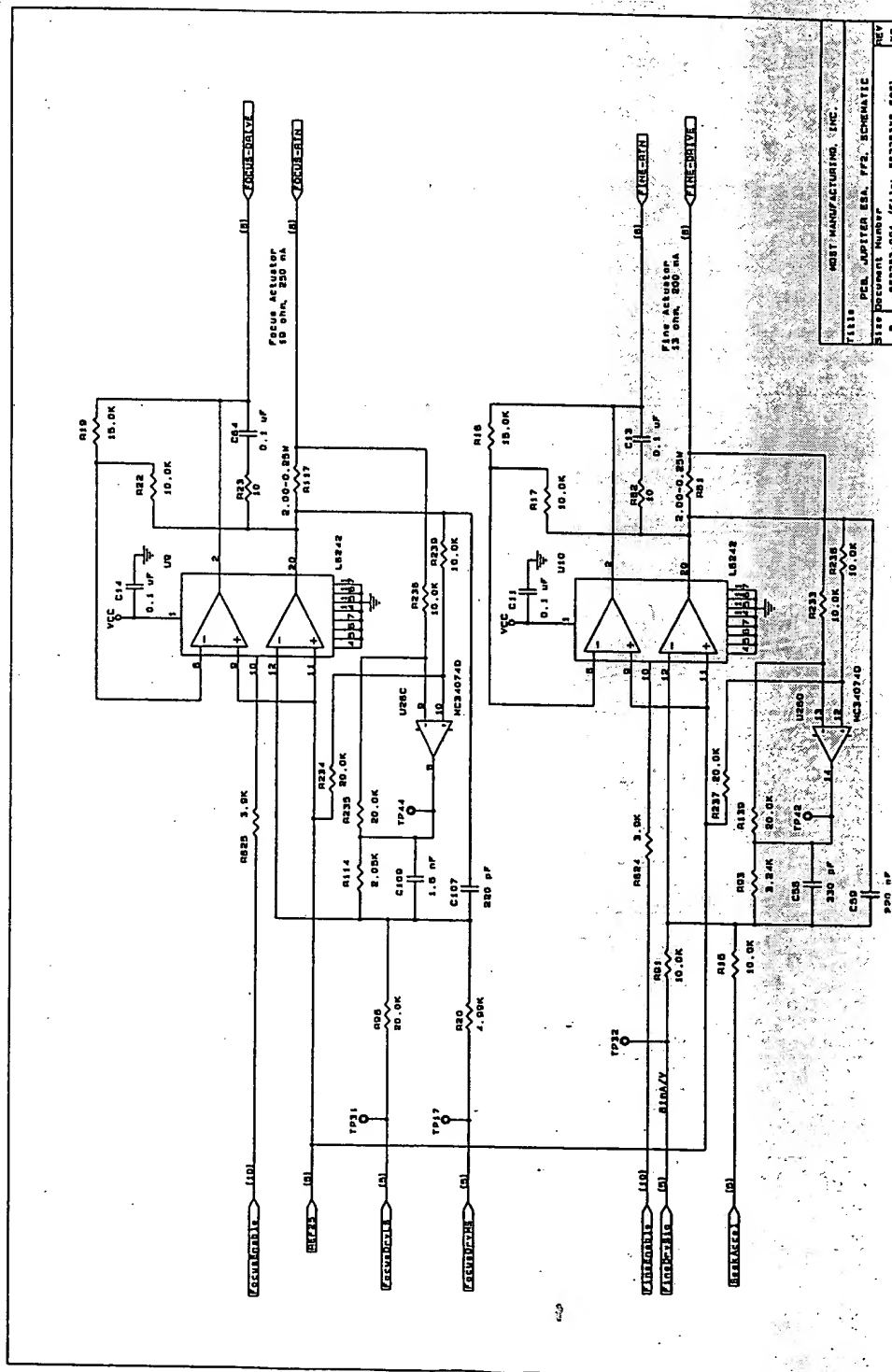
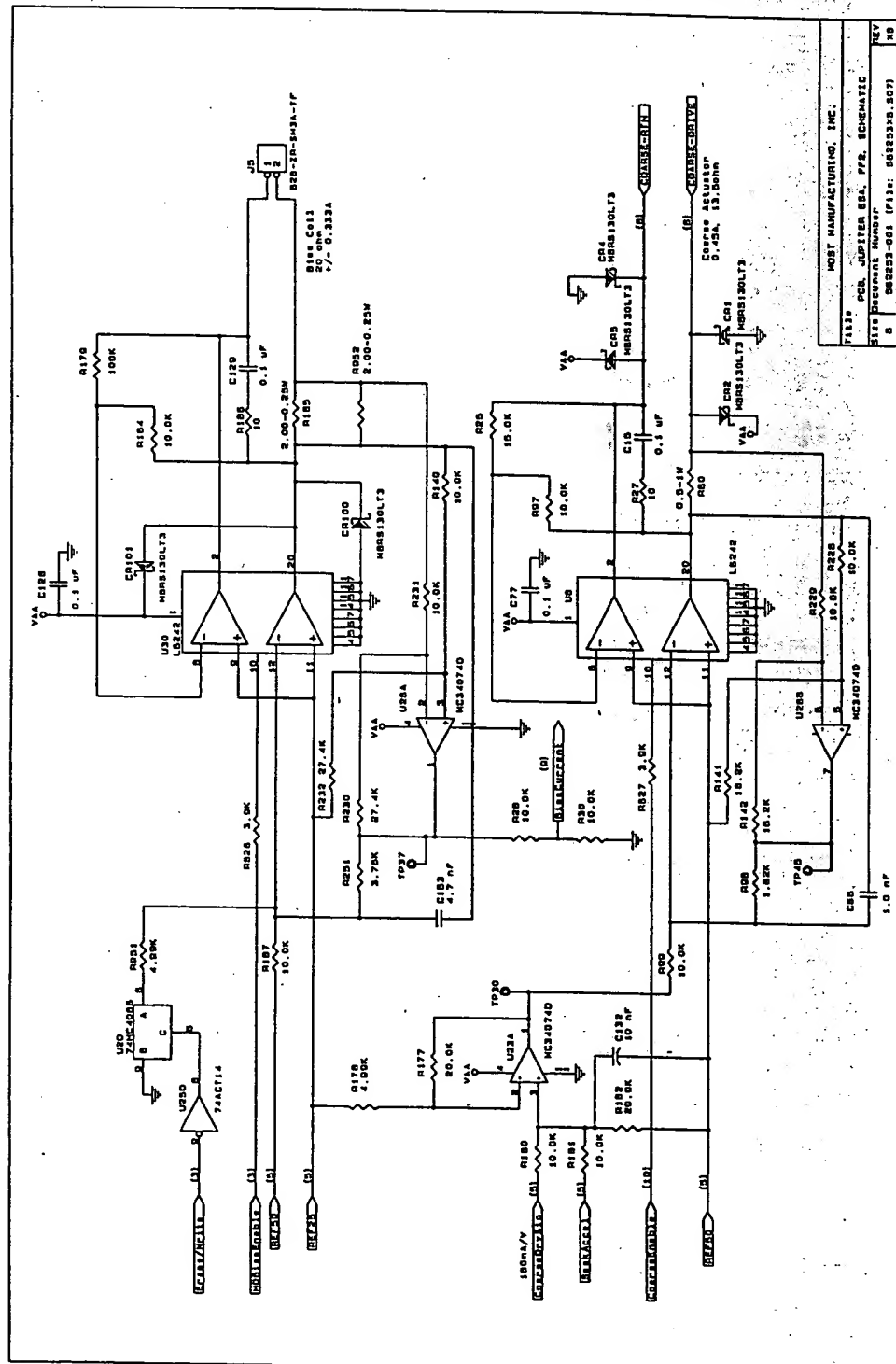


FIG 112



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File	PCB JUPITER E&A, PFB, SCHEMATIC	Document Number	Size	Rev
8	002253-001 (File: 002253XB.S08)			X8

The schematic diagram illustrates the internal circuitry of the PFE (Pulse Frequency Encoder) module, showing the interconnection of various integrated circuits and passive components.

Key Components and Connections:

- U1 (74180):** A 4-bit binary decoder. Its inputs (A0-A3) are connected to address lines 15-18. Its outputs (Y0-Y7) are connected to data lines 1-8. It also receives control signals from lines 9-14.
- U2 (74180):** Another 4-bit binary decoder, similar to U1, with inputs connected to address lines 15-18 and outputs to data lines 9-16.
- U3 (74180):** A third 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 17-24.
- U4 (74180):** A fourth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 25-32.
- U5 (74180):** A fifth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 33-40.
- U6 (74180):** A sixth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 41-48.
- U7 (74180):** A seventh 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 49-56.
- U8 (74180):** An eighth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 57-64.
- U9 (74180):** A ninth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 65-72.
- U10 (74180):** A tenth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 73-80.
- U11 (74180):** An eleventh 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 81-88.
- U12 (74180):** A twelfth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 89-96.
- U13 (74180):** A thirteenth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 97-104.
- U14 (74180):** A fourteenth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 105-112.
- U15 (74180):** A fifteenth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 113-120.
- U16 (74180):** A sixteenth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 121-128.
- U17 (74180):** A seventeenth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 129-136.
- U18 (74180):** An eighteenth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 137-144.
- U19 (74180):** A nineteenth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 145-152.
- U20 (74180):** A twentieth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 153-160.
- U21 (74180):** A twenty-first 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 161-168.
- U22 (74180):** A twenty-second 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 169-176.
- U23 (74180):** A twenty-third 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 177-184.
- U24 (74180):** A twenty-fourth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 185-192.
- U25 (74180):** A twenty-fifth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 193-200.
- U26 (74180):** A twenty-sixth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 201-208.
- U27 (74180):** A twenty-seventh 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 209-216.
- U28 (74180):** A twenty-eighth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 217-224.
- U29 (74180):** A twenty-ninth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 225-232.
- U30 (74180):** A thirtieth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 233-240.
- U31 (74180):** A thirty-first 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 241-248.
- U32 (74180):** A thirty-second 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 249-256.
- U33 (74180):** A thirty-third 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 257-264.
- U34 (74180):** A thirty-fourth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 265-272.
- U35 (74180):** A thirty-fifth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 273-280.
- U36 (74180):** A thirty-sixth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 281-288.
- U37 (74180):** A thirty-seventh 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 289-296.
- U38 (74180):** A thirty-eighth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 297-304.
- U39 (74180):** A thirty-ninth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 305-312.
- U40 (74180):** A fortieth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 313-320.
- U41 (74180):** A forty-first 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 321-328.
- U42 (74180):** A forty-second 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 329-336.
- U43 (74180):** A forty-third 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 337-344.
- U44 (74180):** A forty-fourth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 345-352.
- U45 (74180):** A forty-fifth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 353-360.
- U46 (74180):** A forty-sixth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 361-368.
- U47 (74180):** A forty-seventh 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 369-376.
- U48 (74180):** A forty-eighth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 377-384.
- U49 (74180):** A forty-ninth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 385-392.
- U50 (74180):** A fiftieth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 393-400.
- U51 (74180):** A fifty-first 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 401-408.
- U52 (74180):** A fifty-second 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 409-416.
- U53 (74180):** A fifty-third 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 417-424.
- U54 (74180):** A fifty-fourth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 425-432.
- U55 (74180):** A fifty-fifth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 433-440.
- U56 (74180):** A fifty-sixth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 441-448.
- U57 (74180):** A fifty-seventh 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 449-456.
- U58 (74180):** A fifty-eighth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 457-464.
- U59 (74180):** A fifty-ninth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 465-472.
- U60 (74180):** A sixtieth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 473-480.
- U61 (74180):** A sixty-first 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 481-488.
- U62 (74180):** A sixty-second 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 489-496.
- U63 (74180):** A sixty-third 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 497-504.
- U64 (74180):** A sixty-fourth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 505-512.
- U65 (74180):** A sixty-fifth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 513-520.
- U66 (74180):** A sixty-sixth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 521-528.
- U67 (74180):** A sixty-seventh 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 529-536.
- U68 (74180):** A sixty-eighth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 537-544.
- U69 (74180):** A sixty-ninth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 545-552.
- U70 (74180):** A seventieth 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 553-560.
- U71 (74180):** A seventy-first 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 561-568.
- U72 (74180):** A seventy-second 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 569-576.
- U73 (74180):** A seventy-third 4-bit binary decoder, with inputs connected to address lines 15-18 and outputs to data lines 577-584.

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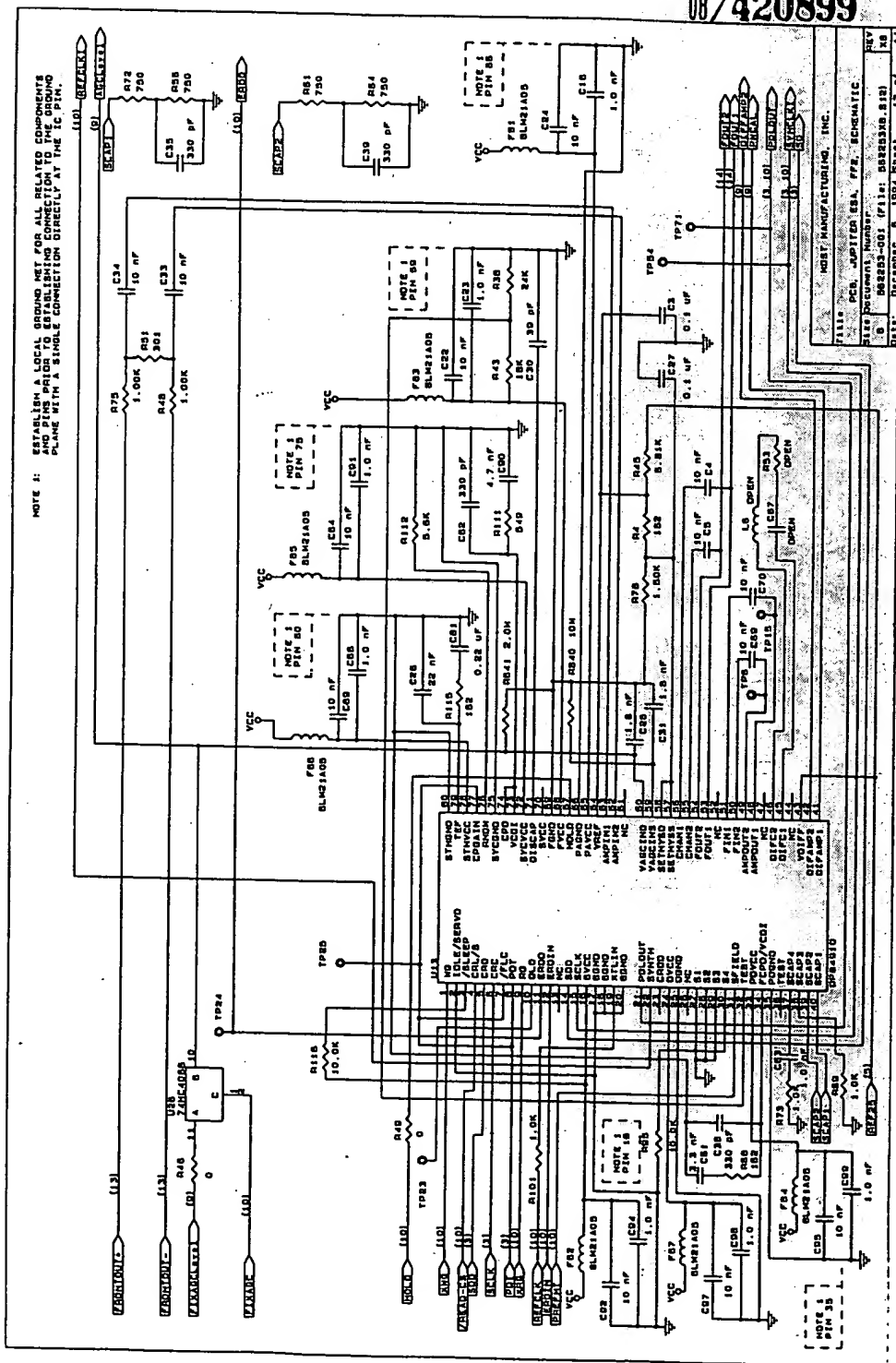
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FILE#	PCB, JUPITER SEA, FPD, SCHEMATIC	REV
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MOSBY MANUFACTURING, INC.		

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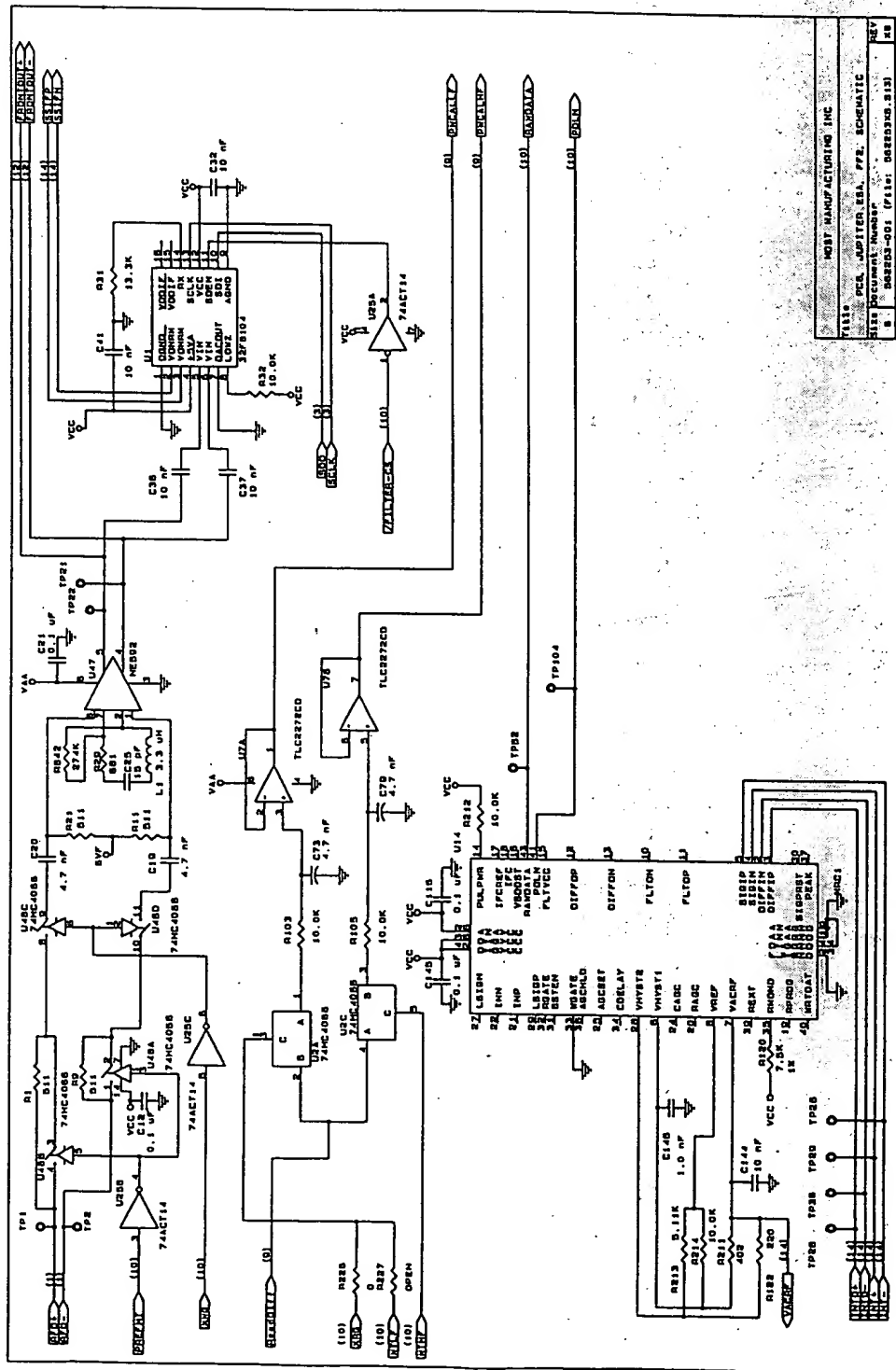
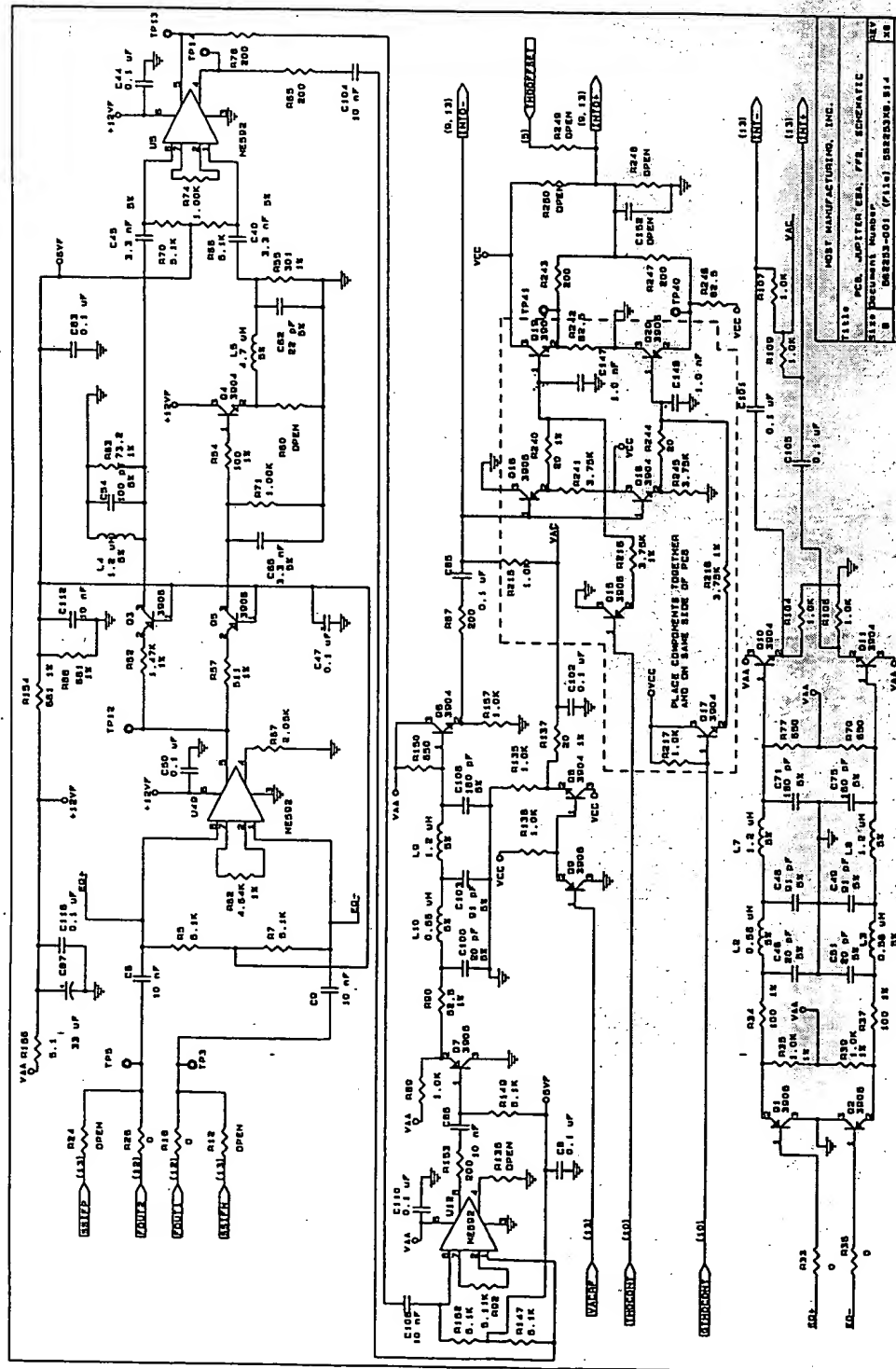


FIG. 119



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CRASH STOP/POLE-PIECE ISOLATOR 8/18/93 MD

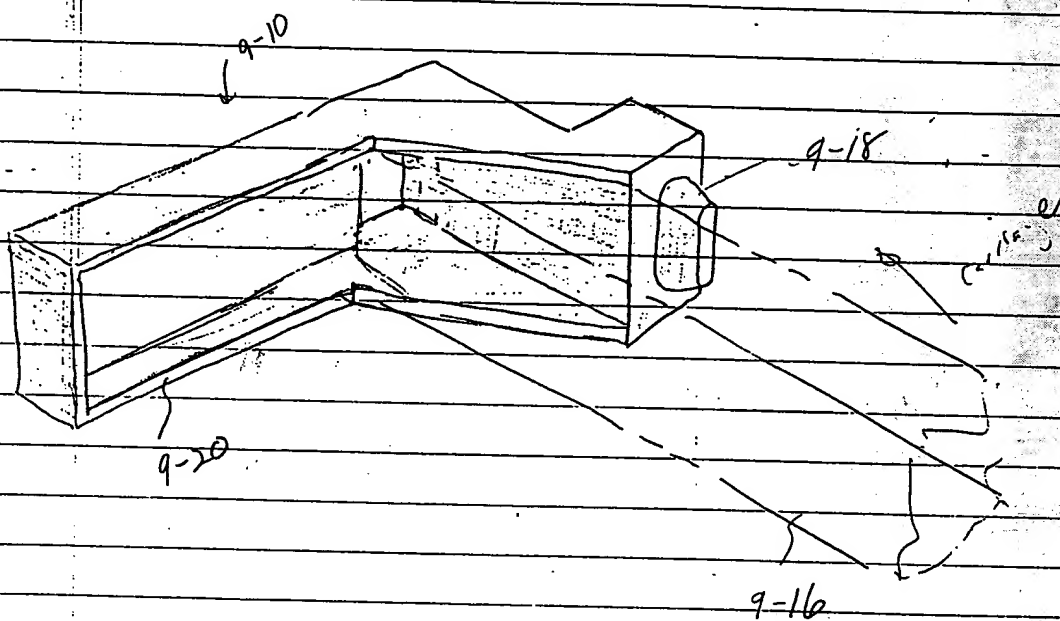


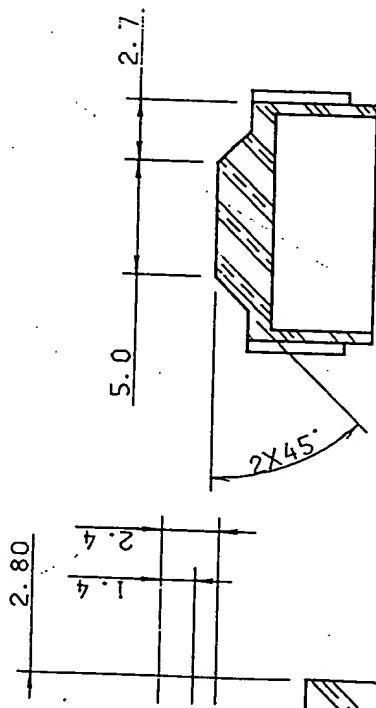
FIG. 120

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SECTION B-B

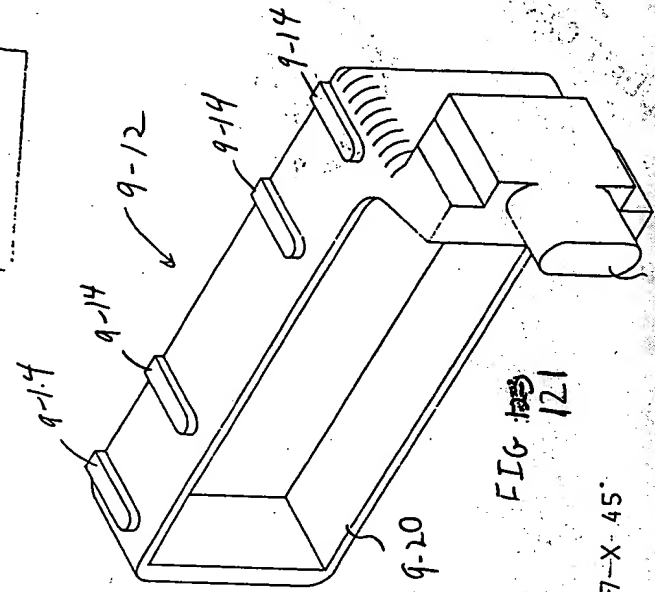
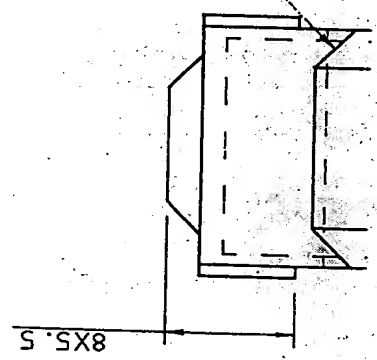
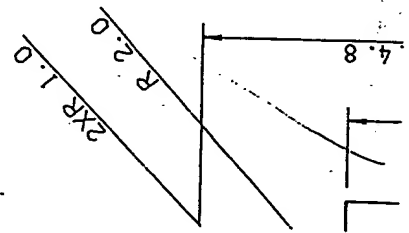


FIG. 121

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